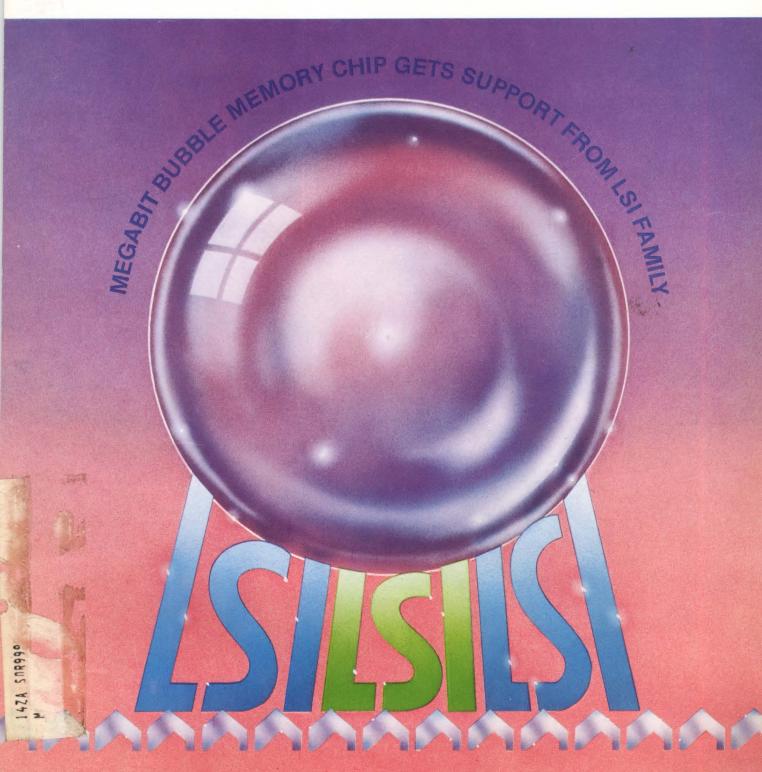
APRIL 26, 1979

SPECIAL REPORT: HERE COME THE FAST STATIC RAMS/125

Hybrids, materials dominate components conference / 112 Single chip interfaces IEEE-488 bus in measurement systems / 145







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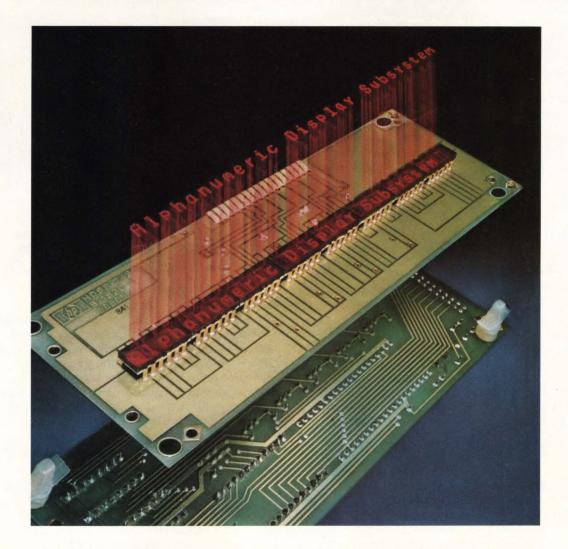
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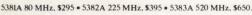
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Electronics

The International Magazine of Electronics Technology



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Highlights

Cover: LSI aids bubble memory design, 105

Ease of use could determine which bubble memories succeed best with designers. So a new megabit bubble memory comes complete with a group of circuits that will interface it to many different systems.

Cover is by Sean Daly.

Look, no central processing unit, 92

A radically different computer architecture from the Massachusetts Institute of Technology has hundreds of arithmetic and logic units processing parts of a problem simultaneously and using packet-switching to route the results through similarly decentralized memory units.

Hybrids inherit ECC, 112

In a marked shift of emphasis, this year's Electronic Components Conference is focussing on materials, manufacturing methods, and packaging, particularly hybrid packaging of very large-scale integration, says this ECC preview. Also worth noting are some novel hybrid circuits and work on gallium-arsenide field-effect transistors.

Static RAMs pick up speed, 125

Led by Fairchild and Intel, makers of 4-K static random-access memories are pushing access times below 55 nanoseconds. This special report describes these rapidly expanding options for fast cache and buffer memories.

. . . and in the next issue

A special report on data converters . . . a magnetic-bubble memory tester . . . replacing backplanes with zero-insertion-force connectors.

Electronics

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Publisher's letter

t is always exciting to print a story that can shake up the industry—for instance, the cover article in this issue (p. 105), on the development of the 1-megabit magnetic-bubble memory and support chips at Intel Corp.'s subsidiary, Intel Magnetics Inc., Santa Clara, Calif.

Written by vice president of engineering Dick Clover, product engineer Dave Lee, and bubble memory marketing manager Don Bryson, the technical article is the first general disclosure of this group of products. In fact, when arranging for the piece, solid state editor Ray Capece and San Francisco regional bureau manager Bill Arnold were the first editors ever to have been allowed to tour the closely guarded Intel Magnetics facility.

To ready the memory and support chips for market took the combined efforts of the magnetics subsidiary and two Intel divisions. The Special Products division worked on the bipolar Schottky current-pulse generator and the complementary metal-oxide-semiconductor coil predrivers. The Microcomputer Components division was responsible for the n-channel formatter/sense amplifier and the HMOS bubble memory controller.

Without these integrated control and driver circuits, there wouldn't be much of a product. As Bryson points out, "Give somebody a bubble memory and not a heck of a lot can be done with it without support chips to make it run."

Now that bubble memories have been made easy for users to apply, products using them should be on the market within a year, Intel esti-

mates. "Ahead we can see a path similar to that of dynamic randomaccess memories—a quadrupled capacity in three years, to 4 megabits and then 8 megabits," Bryson states.

f someone were to ask you what components are operating as frontend amplifiers for communications satellites and you were aware of the latest technology, you might answer gallium-arsenide field-effect transistors. Right? Wrong.

On a recent visit to the ComSat Laboratory in Bethesda, Md., communications editor Harvey Hindin was dumbfounded to discover that the birds are flying around up there with tunnel diodes aboard, though the devices were originally developed some 20 years ago.

"I had to find out why," says Harvey, and he was intrigued enough with the answer to produce the Probing the News on page 81.

The reason turned out not to be nostalgia, but the reliability ensured by new preflight screening procedures. So far, over 100 tunnel-diode amplifiers have gone into orbit without a single flight failure.

Nevertheless, these old dependables will probably not be around too much longer, according to Harvey. Eventually the new GaAs FETs will pass tunnel diodes in reliability and offer better noise figures into the bargain, signaling the end for the old timers in this application.

April 26, 1979 Volume 52, Number 9

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Readers' comments

Already ready

To the Editor: I would like to point out a significant omission in your March 15 review of bus-compatible converters ["IC makers ready converters for 8-bit processors," p. 39]. While others talk of introducing such products, AMD has already done so. In fact, last year we introduced a pair of bus-compatible digital-to-analog converters, the Am6080 and Am6081 (see Electronics, Oct. 12, p. 180). These Busdac products contain the data-bus input latches and the address and decoding circuitry that allow them to interface with any 8-bit microprocessor.

> Robert M. Grossman Advanced Micro Devices Inc. Sunnyvale, Calif.

Waste as savings?

To the Editor: The News Update column on March 1 [p. 8] quotes a Federal Aviation Administration lead engineer proudly claiming "great" power savings by revamping plan-view displays at 20 en-route air terminals, for a purchase price of \$1 million. If this is an example of the quality of technical decision-making in a government bureau, it is no wonder our energy policy can't get off the ground.

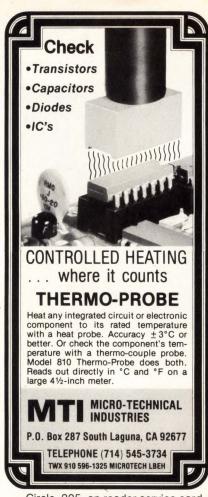
Based on an estimated 20 PVDs in each of the terminals operating continuously, and saving 450 watts each, at an electric utility rate of 5¢ per kilowatt-hour, this "savings" will require more than 12 years to pay out. Since the quoted price probably does not include freight, installation, or the myriad of Government contract overhead costs, I imagine the payout is more likely about 20 years.

Your reporter missed the real story—another example of waste, foisted on the taxpayer and masquerading as Government savings!

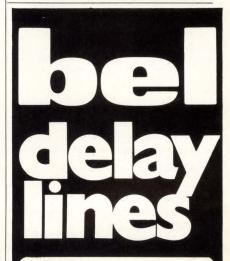
J. W. Pehoushek Cincinnati, Ohio

Correction

That new line of Regent terminals, Regent 300 terminal cluster system and System 75 (April 12, p. 42) is, of course, from Applied, not Advanced, Digital Data Systems Inc.



Circle 225 on reader service card



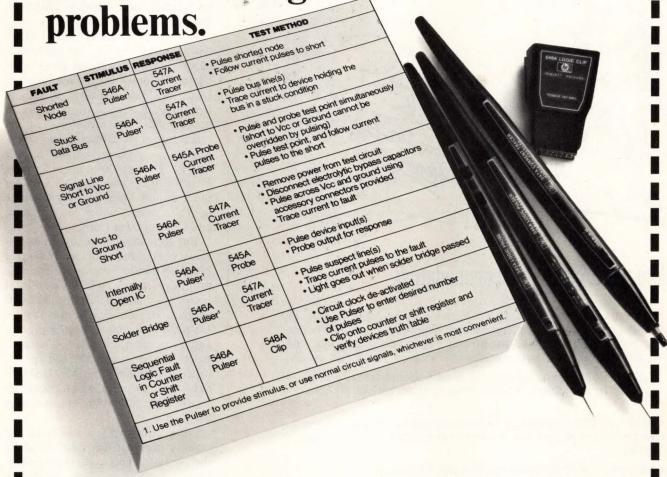
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News update

■ No one can accuse the military of moving with unseemly haste to purchase electronic systems. A case in point is the Navy's two-year old plan to equip its vessels and aircraft with standard militarized computers, peripherals, and software [Electronics, Dec. 23, 1976, p. 54].

Called the Tactical Digital Standardization Program, the exercise is supervised by the Naval Electronics Systems Command in Washington, D. C., as a means of saving money in training, documentation, maintenance, and parts inventory, among other things. It attracted the attention of such heavyweights as the Sperry Univac division of Sperry Rand Corp., whose AN/UYK-20 minicomputer was the first machine to win approval under the program, and Control Data Corp.

But to a small company in Plainview, N. Y., the Qantex division of North Atlantic Industries Inc., the program represented a potential boon. Qantex supplies the \$20,000 magnetic-tape cartridge unit for the UYK-20 as well as all other present and proposed mini types. The contract for its standardized parts, called by the Navy the AN/USH-26 data-storage peripheral, could be worth \$50 million to Qantex over five years.

Now, after two years of tests, the Qantex part has been approved by the Navy for fleet-wide deployment. Orders have been piling up during that period, although 462 have been shipped, mostly to Navy contractors for use in their system development.

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Joel Kramer, president of Qantex, says the Navy has 50 programs under development that will require tape-storage systems like the model 26.

-Howard Wolff

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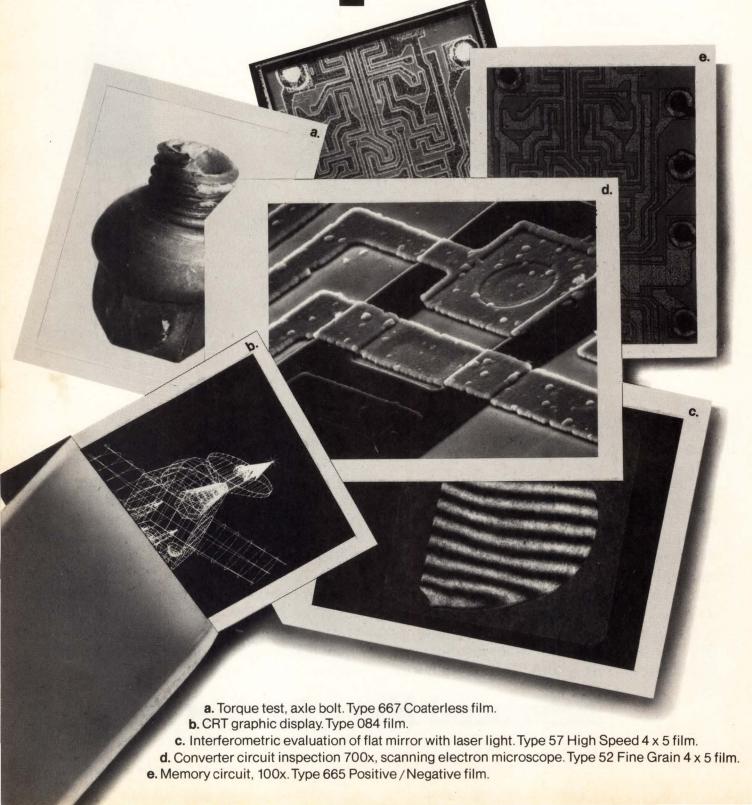
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New, low cost OPTRON LED's offer exceptional light output characteristics in a choice of wide or narrow beam spreads.

OPTRON's new OP 190 and OP 195 plastic encapsulated light emitting diodes give high performance with light output characteristics exceeding the specifications of currently avail-

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The new OP 190 and OP 195 feature a typical power output of 10 mW at 100 mA and are capable of pulsed op-

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The OP 190 has a beam spread of 40° (total angle between half intensity points) and a typical radiant intensity at 100 mA of 15 mW/sr.



OP 195 ACTUAL SIZE

For applications requiring a concentrated beam over longer distance, the OP 195 is designed with a beam spread of only 15° and radiant intensity of 50 mW/sr.

Detailed technical information on these new high reliability, low cost plastic LED's and other OPTRON optoelectronic products is available from your nearest OPTRON sales representative or the factory direct.



People

Biomation's Blecki revels in high-end logic analyzers

Price sensitivity is being thrown to the winds when it comes to buying logic analyzers, says David J. Blecki, 39, recently named president of Gould Inc.'s Biomation division. "Anything you can do to make an engineer's job more efficient in view of the manpower shortage is worth it," he says.

High-end logic analyzers, selling for around \$10,000, are indispensable to the development of busoriented computer systems, he believes. It is the product to which Biomation, a 10-year-old Santa Clara, Calif., maker of waveform recorders and logic analyzers, will devote most of its research and development dollars. Low-end analyzers will come later, he says, after designers develop specific needs.

Strength. Blecki, with a master's degree in electrical engineering and eight years under his belt as Biomation's marketing vice president, takes over a company in a strong position. Running third in the logic analyzer market—total sales were \$50 million in 1978-behind leader Hewlett-Packard, for whom he once worked, and runner-up Tektronix until last September, Biomation moved to a "solid No. 2," Blecki says, mostly because of the success of its model K100-D, which was introduced then.

The 20-input, 100-megahertz analyzer, with a variety of display formats, has taken the market by storm, he maintains. "We've had a step-function increase in market share because of that product." Moreover, it pulled Biomation, which had grossed \$9 million before being acquired in 1977 by Gould, out of a slump.

Of the field-service market, Blecki says the logic analyzer may be a bit of overkill there. "A logic analyzer reveals a lot of information about a system that requires a highly skilled technician to interpret."

In theory, smarter instruments that relieve the need for technician interpretation have merit, he says, but they require too much software



Worthwhile. A price of \$10,000 is little enough to pay to make an engineer more efficient, says David Blecki.

support. "Right now, the only widely accepted field service technique continues to be board exchange.'

Now that he is at the helm, Blecki regrets he has to delegate all the "fun stuff" and take on the problems "with no solution." One of the first he must grapple with, he says, is President Carter's voluntary 7% wage ceiling. "How do you stay within 7% when in this area 20% isn't enough to keep a technician in your employ?" asks Blecki.

Schineller moves MAI toward the electronic office

Sights focused sharply on the office of the future, Richard J. Schineller is moving his company, Management Assistance Inc., smartly in that direction. Word processing is a key, says the 44-year-old executive vice president for domestic operations.

At the Interface 79 data communications show in Chicago earlier this month, MAI unveiled part of what he has in mind: word-processing capabilities in a data-processing network, a new feature of the Data-Word system introduced a few months ago by subsidiary Basic Four Corp. With 1978 sales of \$119 million out of MAI's \$200 million, Basic Four has catered to the smallbusiness computer user.

Now Schineller wants to provide word processing for this same mar-



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This new system is based on Cromemco's well-known System Three Computer and our new Multi-User BASIC software package.

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- No round-off error in financial work (because our BASIC uses binarycoded decimal rather than binary operation). And we've still been able to make it FAST.
- Terminals and printer are interruptdriven — no additional overhead until key is pressed.
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Booth No. 330 at the SID Show.

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People



New fields. Richard Schineller might even consider computerized branch exchanges.

ket. "What we introduced [in Chicago] was improved distributed dataprocessing capacity with implications for electronic mail," he says.

He has plans for all three MAI subsidiaries. The others are Wordstream Corp., with word-processing systems for larger companies than those Basic Four serves, and Sorbus Inc., a computer-service company, where he plans expansion in the area of word-processing equipment.

Schineller has been watching the development of the electronic office since his 1956-65 stint with IBM. From there he went to MAI, head-quartered in New York, for three and a half years in its days as a purchase and lease-back company. After brief stays at two other firms, he returned to MAI when it started Basic Four and Sorbus in 1971—first as vice president for business planning and develoment and then in his present position.

Plans. Basic Four will continue to add capabilities to its office systems, as the Interface 79 introduction suggests, he says. And plans are even more ambitious at Wordstream. Look for an electronic alternative to the file cabinet, Schineller says, as well as electronic mail handling.

Another important role could be integration of the entire communications management function. Management of communications could become as important a factor in MAI's product lines as management of data and text, he says.

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Signetics' new dual op amps. Team them with your design for the industry's lowest noise.

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NE5533	Low Noise: 4.5nV/√Hz (max.); 200kHz power BW @ 13V/µsec slew.				
NE/SE5530*	High Slew: 35V/µsec; internally compensated; 500kHz power BW; 3MHz small-signal BW.				
NE/SE5535*	High Slew: 15V/μsec; internally compensated; 200kHz power BW; 1MHz small-signal BW.				
NE/SE5538*	High Slew: $60V/\mu$ sec; compensated to gains of $+5/-4$; 700kHz power BW; 6MHz small-signal BW.				

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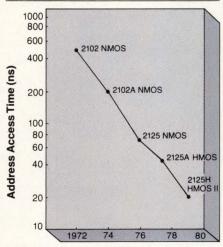


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Intel introduces HMOS II* and a new family of static RAMs that cross the finish line in 20 ns.

Intel just set a new pace for high performance memory with HMOS II. It's our patented next generation MOS technology so advanced it delivers speeds faster than bipolar and even our own first generation HMOS process. HMOS II gives designers the fastest, lowest power static RAMs ever—plus traditional MOS economy and reliability. Our new

History of MOS speed



Intel's continued process and scaling improvements have doubled MOS speeds every two years. The above graph demonstrates this trend with Intel's 1K x 1 static RAMs.

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2147H-1	35	180	30
2147H-2	45	180	30
1024x1**			
2125H-1	20	125	
2115H-2	25	125	
2125H-2			
2115H-3 2125H-3	30	100	
2115H-4 2125H-4	35	125	

*Over full 0° to 75°C operating temperature range.

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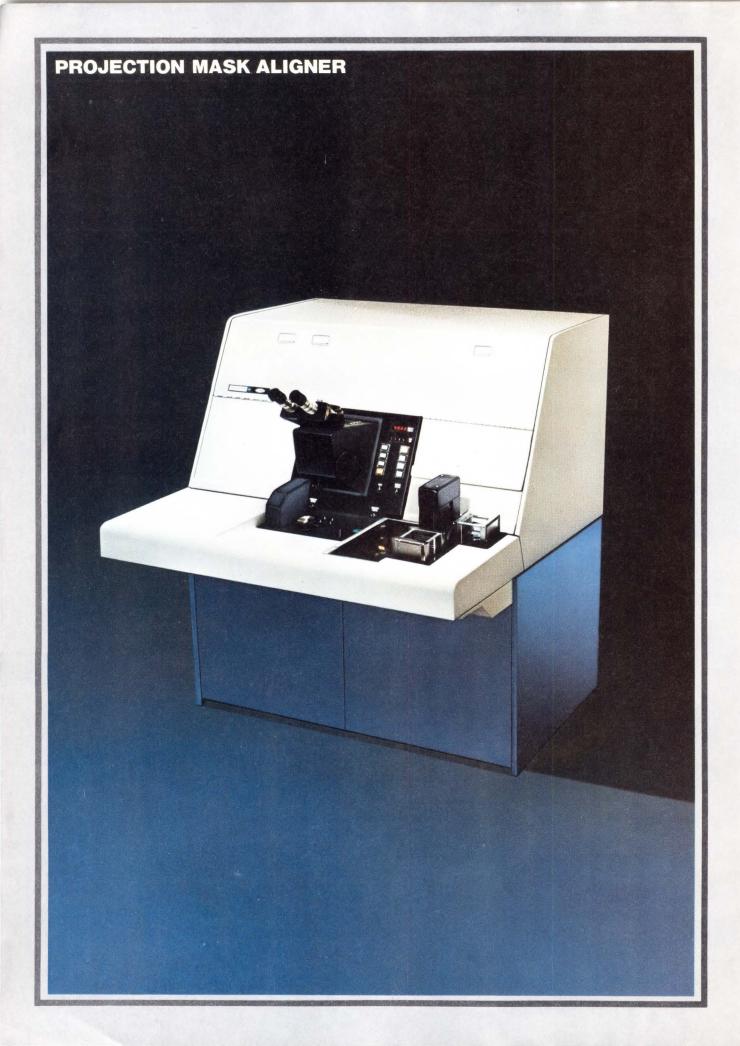
If you envision use of fiber optics in your computer system, telecommunications, industrial applications, or for any other purpose, write us on your letterhead. Because we may already have

gone over the same ground. And because we both know the optical fiber communications age has begun.

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ELECTRO-OPTICAL PRODUCTS DIVISION

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Introducing the Micralign 200 Series. Higher throughput than step-and-repeat at a much lower price.

Perkin-Elmer designed the new Micralign Model 200 to be the most cost-effective projection mask aligner available. In performance, it achieves 2-micron geometries or better in production, distortion/magnification tolerance of 0.25 micron, and 4 percent uniformity of illumination. Options available include automatic wafer loading and automatic alignment to 0.25 micron. Soon to be available: deep UV optical coatings for still smaller geometries.

Compared to the leading stepand-repeat aligner, the Micralign Model 200 delivers outstanding performance for not much more than half the cost. It takes about a quarter of the floor space. It provides consistently higher throughput regardless of die size.

The Model 200's remarkable performance is the result of a number of major innovations.

Improved optical design and fabrication

We improved the optical design to provide increased resolution

and depth of focus. Optical manufacturing tolerances are five times tighter to ensure precise overlay from aligner to aligner.

Near-zero vibration

We minimized vibration. We constructed the Model 200 with two frames—one inside the other. The inner frame, which carries the projection optics and carriage drive, is completely isolated from the outer frame.

We incorporated a superb linear motor carriage drive with air bearing slide. This drive does more than eliminate vibration. With the air bearing feature there's no contact and no wear. And no limit to carriage drive durability.

Built-in environmental control

We provided the Model 200 with a built-in environmental chamber. External air, supplied by you or from our optional air conditioning system, is blown through a HEPA filter and heating elements built into the Model 200 top cover. A positive-pressure, class 100 environment is carefully controlled to better than 1°F.

We included a separate thermal control for the mask, to compensate for mask run-out.

No mask contamination

We designed a sealed mask carrier for the Model 200. You put the mask in the special carrier right in the mask department. Seal it. When you load the sealed carrier in the Model 200, the cover plates are automatically removed. After use, the cover plates are automatically replaced.

Proven production capabilities
Perkin-Elmer, the leader in projection mask alignment systems,
offers six years of proven production capability, with an excellent
training and service record.

Get all the facts

These are just a few of the features that make the Micralign Model 200 Series a completely new concept in projection mask aligners. Get more details on how these and other improvements in design can translate into improvements in your production. For literature, write Perkin-Elmer Corporation, Electro-Optical Division, 50 Danbury Road, Wilton, CT 06897. Or phone (203) 762-6057.

Does NTT's chief have his hand on the doorknob?

Representatives of the industrial nations of the world have consummated five years of hard bargaining with an agreement to liberalize world trade. Although individual governments must still ratify the accord reached at Geneva, the pact brings into sharper relief the battle by the United States Government, allied with American telecommunications suppliers, to liberalize an extremely attractive market closed to them until now: Japan's giant Nippon Telegraph and Telephone Public Corp.

What started as a cloud on the horizon has developed into a major diplomatic storm. Sitting at its center is Tokuji Akikusa, president of NTT, who is still firmly resisting the pressure and arm-twisting of the Americans. However, in a recent interview with a Japanese newspaper, Akikusa intimates NTT may eventually back down; his thinking is that his company will have to agree to some concessions—beyond those already offered in the way of open procurement of such items as telephone poles—because it simply cannot expect to have its way in all areas.

Akikusa makes the point that even if his utility were to buy \$3 billion worth of equipment from overseas suppliers, "it will take 10 years to carry this out. . . . It will be impossible to completely revise the present procurement method." The company president also addresses the broader problem of virtual subsidization by NTT of a supplier network, a so-called inner circle, and its responsibility to ensure solvency of the members of that circle.

"Once an enterprise enters that inner circle," he says, "NTT must look after the enterprise on a permanent basis. There will be a loss from a national economic point of

view if the NTT tells an enterprise that has built big plants and trained technicians that its services are no longer required."

Asked if it were something of an exaggeration to say that opening NTT's procurement to foreign suppliers would cause a chain reaction of Japanese bankruptcies and unemployment, Akikusa replies, "If a competitive bidding system is introduced, there are fears that know-how developed by experts after much [effort] will be released outside. The technicians will lose their [incentive] to work if know-how developed not only by the NTT but also by [its suppliers] is made available. Enterprises connected with the corporation will not go bankrupt one after the other. But Nippon Electric Co. [for example], relies on the NTT for around 20% of its orders, and Fujitsu Ltd. 22% to 23%. There are also firms engaged only in producing equipment for the NTT. Such firms will suffer most."

Does Akikusa think that behind the open-door demand of the U. S. is a plan by IBM and other American computer makers to "cultivate" the Japanese market? "There appears to be such a rumor," Akikusa replies, "but there is no definite proof. . . . The communications business does not merely involve telephones and telegraph. It probably will nurture all sorts of industries in the future. Therefore I believe the American side is also aware that the communications business has big future possibilities in respect to industrial strategy."

But Akikusa's closing words, which reflect the long decision-making process in Japan, could be the most prophetic. "I would like," he said, "to open doors gradually."

The Microcomputers you should take seriously.

The C3 Series is the microcomputer family with the hardware features, high level software and application programs that serious users in business and industry demand from a computer system, no matter what its size.

Since its introduction in August, 1977, the C3 has become one of the most successful mircocomputer systems in small business, educational and industrial development applications. Thousands of C3's have been delivered and today hundreds of demonstrator units are set up at systems dealers around the country

Now the C3 systems offer features which make their performance comparable with today's most powerful minibased systems. Some of these features

Three processors today, more tomorrow.

The C3 Series is the only computer system with the three most popular processors- the 6502A, 68B00 and Z-80. This allows you to take maximum advantage of the Ohio Scientific software library and the tremendous number of programs offered by independent suppliers and publishers. And all C3's have provisions for the next generation of 16 bit micros via their 16 bit data BUS, 20 address bits, and unused processor select codes. This means you'll be able to plug a CPU expander card with two or more 16 bit micros right in to your existing C3 computer.

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Five DOS options including development, end user, and virtual data file single user systems, real time, time share, and networkable multi-user systems.

languages including three types of BASIC

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plus FORTRAN and COBOL with more languages on the way. And, of course, complete assembler, editor, debugger and run time packages for each of the system's microprocessors.

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OS-DMS, the new software star.

Ohio Scientific has developed a remarkable new Information Management system which provides end user

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intelligence far beyond what you would expect from even the most powerful minisystems. Basically, it allows end users to store any collection of information under a Data Base Manager and then instantly obtain information, lists, reports, statistical analysis and even answers to conventional "English" questions pertinent to information in the Data Base. OS-DMS allows many applications to be computerized without any programming!

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Ohio Scientific now offers the 6502C microprocessor with 150 nanosecond main memory as the GT option on all C3 Series products. This system performs a memory to register ADD in 600 nanoseconds and a JUMP (65K byte. range) in 900 nanoseconds. The system performs an average of 1.5 million instructions per second executing typical end user applications software (and that's a mix of 8, 16 and 24 bit instruc-

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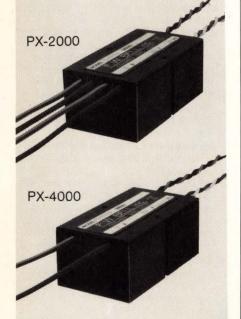
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Meetings

25th International Instrumentation Symposium, Instrument Society of America, Sheraton Hotel, Anaheim, Calif., May 7–10.

ISS '79—International Switching Symposium, Colloque International de Commutation (Paris), PLM St. Jacques Hotel, Paris, May 7–11. For information in the U.S., contact A.E. Joel Jr., Bell Laboratories, Holmdel, N. J.

1979 SID International Symposium, Society for Information Display (Los Angeles), Chicago Marriott Hotel, Chicago, May 7-11.

29th Electronic Components Conference, EIA and IEEE, Hyatt House, Cherry Hill, N. J., May 14–16.

Electrical and Electronic Measurement and Test Instrument Conference, IEEE, Skyline Hotel, Ottawa, May 15–17.

Naecon—National Aerospace and Electronics Conference, IEEE and Naecon (Dayton, Ohio), Dayton Convention Center, May 15-17.

Advances in Systems Technology: Trends and Applications, 1979, IEEE and NBS, National Bureau of Standards, Gaithersburg, Md., May 17.

Huntsville Electro-Optical Technical Symposium and Workshop, Society of Photo-Optical Instrumentation Engineers (Bellingham, Wash.), Huntsville Hilton, Huntsville, Ala., May 22–25.

Failure Avoidance Seminar, Integrated Circuit Engineering Corp. (Scottsdale, Ariz.), Hilton Inn, Jamaica, N. Y., May 23-24.

Conference on Laser Engineering and Applications, IEEE and Optical Society of America, Washington Hilton Hotel, Washington, D. C., May 30-June 1.

Computers in Communications Conference, American Institute of Aeronautics and Astronautics (Los Angeles), International Inn, Washing-

ton, D. C., May 31-June 1. Program will be repeated at the Hyatt L. A. International Hotel, Los Angeles, June 25-26.

1979 International Summer Consumer Electronics Show, EIA, McCormick Place, Chicago, June 3–6.

NCC '79—1979 National Computer Conference, IEEE, American Federation of Information Processing Societies, New York Hilton and Americana Hotels, New York, June 4–7.

Automated Testing for Electronics Manufacturing, Benwill Publishing Co. (Boston), Radisson Ferncroft Hotel, Danvers, Mass., June 4–7.

ICC '79—International Conference on Communications, IEEE, Sheraton Boston Hotel, Boston, June 11–14.

Machine Vision, Automatic Assembly, and Productivity Technology, summer session, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, MIT, Cambridge, Mass., June 11–15.

33rd Annual Convention of the Armed Forces Communications and Electronics Association, AFCEA (Falls Church, Va.), Sheraton Park Hotel, Washington, D.C., June 19-21.

Device Research Conference, IEEE, at the University of Colorado, Boulder, Colo., June 25-27.

Second Joint Intermag—Magnetism and Magnetic Materials Conference, IEEE and American Institute of Physics, Statler Hilton Hotel, New York, July 17–20.

Compcon Fall '79—18th IEEE Computer Society International Conference, IEEE, Capital Hilton Hotel, Washington, D. C., Sept. 4–7.

Second International Fiber Optics and Communications Exposition, Information Gatekeepers Inc. (Brookline, Mass.), Hyatt Regency O'Hare Hotel, Chicago, Sept. 5–7.

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So ours let you sample synchronously and asynchronously.



Use the 7D01F for hardware and software applications.

As a digital designer you must be versatile enough to do the entire design job. Logic and timing. Software and hardware analysis. Activity on and off the bus.

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Synchronous and asynchronous sampling: it helps

make our Logic Analyzers versatile. So you can do to-day's job and tomorrow's. So you can change applications without changing your logic analyzer.

Contact Tektronix Inc., P.O. Box 500, Beaverton, OR 97077. In Europe, Tektronix, Ltd. P.O. Box 36, St. Peter Port Guernsey, Channel Islands.



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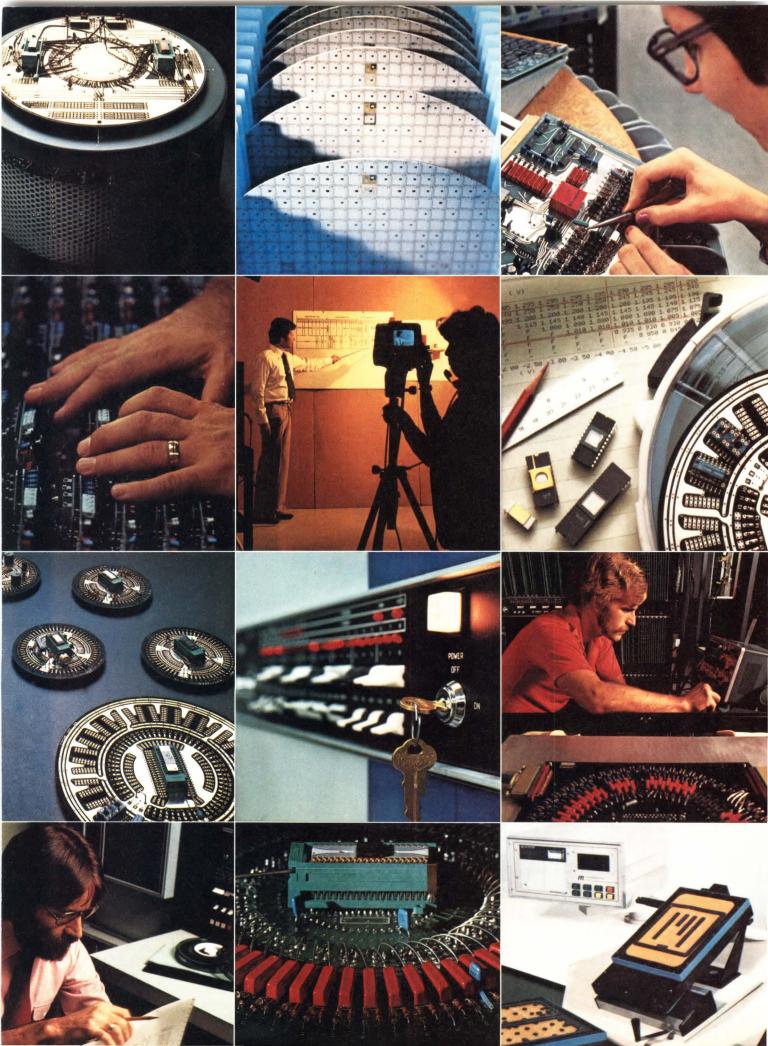
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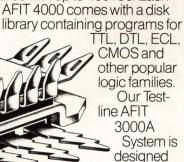
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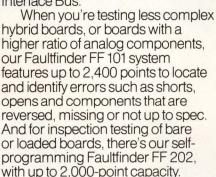


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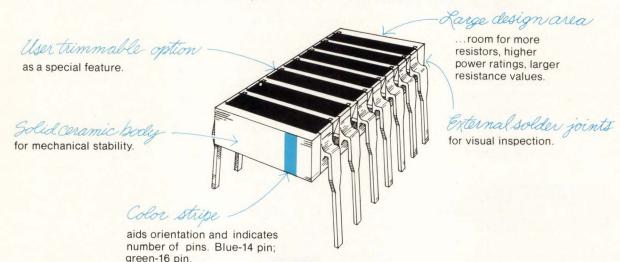
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Pinout of unreleased pseudostatic RAM from Mostek changed

Despite a formal announcement and release of price information last January, Mostek Corp. of Carrollton, Texas, has not yet shipped samples of its MK4816 dynamic random-access memory and has revised the pinout for the device. With preliminary specifications released last summer [Electronics, Aug. 7, 1978, p. 33], the 2,048-by-8-bit single-supply part was the first of what are called pseudostatic devices—containing on-chip refreshing circuitry—to be discussed. (Zilog Corp. described plans for a 32-K pseudostatic device earlier this year.) Samples of Mostek's 4816 were expected last November, and then in the first quarter of this year. But because of design revisions to maximize yield, samples will not be available until June, says Sam Young, a Mostek marketing official.

TI sees 17% rise in world markets

Texas Instruments Inc. expects worldwide semiconductor sales in 1979 to reach \$9.6 billion, some 17% more than the figure for 1978. TI president J. Fred Bucy also told the company's annual meeting last week that the market for calculators and learning aids should have relatively little growth: from last year's \$1.8 billion and 82 million units to \$1.9 billion and 84 million units. The Dallas-based firm also announced that its first-quarter sales netted \$720.8 million, up 29% from last year.

National, Zilog to alternate-source byte-wide pseudos

National Semiconductor Corp. and Zilog Corp. have signed a letter of intent to alternate-source each other with a family of 8-bit-wide pseudo-static random-access-memory chips. The move is seen as a way for both companies to beat Mostek Corp. to the market for byte-wide pseudostatic memories. National, in Santa Clara, Calif., will receive tooling and technical information from Zilog, in nearby Cupertino, for the Z6132, a 4-K-by-8-bit RAM. They will also coproduce and identically specify a 2-K-by-8 and an 8-K-by-8 RAM.

Math processor may be next in 8086 family

The power of Intel Corp.'s 16-bit microcomputer family obviously is not going to come from the 8086 central processing unit alone: the Santa Clara, Calif., company plans a wide range of high-performance support chips to relieve the CPU of its computing burdens. So far, Intel has announced an input/output channel processor called the 8089, and its next may be a high-speed floating-point arithmetic processor called the 8087. This also may be the first IC to meet the IEEE Computer Society's proposed standard for floating-point math. The standard is nearing a detailed specification, and Intel has recently played an important role in refining its definition. Since the 8087 is being designed to work closely with the 8086, it is called a coprocessor.

Specialized terminals share industrial processing chores

Specialized terminals and software are key features of a pair of plant-management systems from Honeywell Inc.'s United States Information Systems Group in Waltham, Mass. Both offer some distributed data-processing capability. The larger of the two builds on the firm's Level 6 minicomputer; the smaller uses a Honeywell/Incoterm SPD terminal processing unit as a front-end processor for a remote host computer. Three microprocessor-based terminals are common to both systems, as are ruggedized keypad and plasma-display devices.

They would accept data on employee time and attendance, inspection

Electronics newsletter.

reports, inventory, work status, material flow, and work in process. Most of the new software was developed for the Level 6 mini. It includes packages for production scheduling, inventory mangement, and materials requirement planning. The SPD processor is programmed in an extended Basic language aimed at transaction processing. The price of a typical Level 6 system is \$116,660; for an SPD-based system it's \$22,390.

Data General unveils small-business systems at Hanover Fair

Data General Corp. announced its CS/30 microprocessor-based small-business computer systems at West Germany's Hanover Fair last week. Priced from \$22,000 to \$49,000, the CS/30s are aimed at companies with as few as four employees, or operation as distributed processors for larger companies, according to spokesmen for the Maynard, Mass., company. The CS/30 model C1 includes 65,536 bits of MOS main memory, a cathode-ray-tube console and interface, a 10-megabyte disk store, and a receive-only printer. Price is \$21,090. The larger of two CS/30 Model C3 systems has 96 kilobits of MOS main memory, a master CRT console and two displays, two 10-megabyte disks, a 300-line-per-minute printer, synchronous communications capability, and IBM 2780/3780-compatible communications software. It sells for \$49,820. Both systems are programmed in interactive Cobol.

Dataram moves into semiconductor sector with RAM

Long a proponent of bulk magnetic core storage for disk emulation and main memory, Dataram Corp. is introducing its first Bulk Semi memory, offering up to 8 megabytes of semiconductor dynamic random-access memory in a standard rack 15³/₄ inches high. The Cranberry, N. J., firm says it is moving into solid state for bulk storage to get more capacity into a box and to take advantage of the RAM's better cost per bit for large-capacity systems. Also, main memory cycle time will drop sharply: for 36-bit operation, from 1.5 μ s to 600 ns. A 1-megabyte system complete with controller board, power supply, and other peripherals will cost \$17,000 in single quantities and will be electrically compatible with the firm's Bulk Core modules, which continue in production. The new line will use 16-K 4116 RAMs, as will the new 128-kiloword DR-113S, a single-board add-on memory for the LSI-11/23. In single quantities, the 16-bit version costs \$31.50, and the 18-bit parity version \$33.50.

TI eschews single-supply 16-K RAM market

Though Texas Instruments Inc. and Motorola Inc. are currently squaring off as the first two firms to supply samples of 64-K dynamic random-access memories requiring only a single 5-V power supply, don't look for a rematch at the 16-K level. TI officials say they don't plan to build a single-supply 16-K RAM soon. The scaled single-supply process developed for TI's 64-K part is just now starting down the learning curve, explains George Robillard, MOS memory marketing manager at TI's Houston operation. "We've a hard time seeing the need for a single 5-V 16-K part at the price we believe it would have to sell to be profitable," he says.

Motorola, on the other hand, is planning to jump into the ring soon with other firms—including Intel, National Semiconductor, and Mostek—that have single-supply 16-K RAMs planned or announced. Peter Bagnall, Robillard's counterpart at Motorola's Austin, Texas, plant, says Motorola expects to have samples of a single-supply 16-K RAM in the third quarter.

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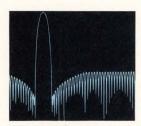


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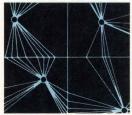
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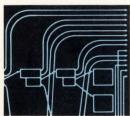


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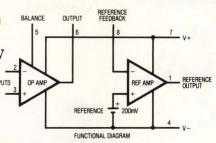
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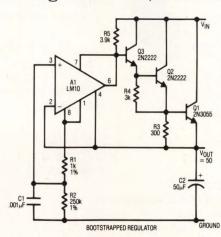
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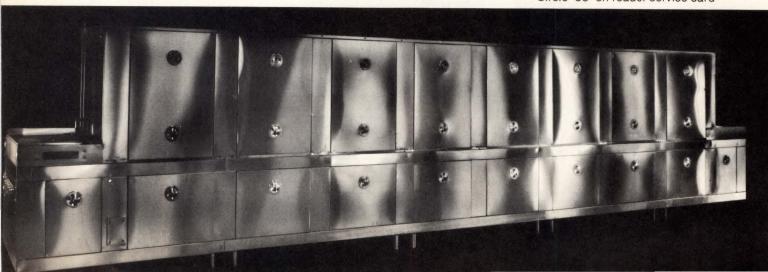
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Japanese boost area, number of LEDs of flat-screen TV

by John Javetski, Consumer & Industrial Editor

Automatic die bonding gives Sanyo a display 160 mm wide, 120 mm high, with 38,400 GaP LEDs

There's no disagreement that the direction TV receivers will take is a flat set that hangs on the wall like a picture. The problem is to find an alternative to the bulky cathode-ray tube. A key firm in that effort, Japan's Sanyo Electric Co., is working with light-emitting diodes, and its latest experimental development is a monochrome receiver that uses no less than 38,400 LEDs in a 160-by-120-millimeter display.

There are a number of possibilities under investigation for the CRT-less set (see "Researching a flat world"). However all prototypes have been plagued by low brightness and resolution and complex manufacturing procedures—problems that Sanyo's research center in Osaka claims to have solved with relatively efficient green gallium-phosphide LEDs and an automated fabrication technique.

Manufacture. In making gallium-phosphide wafers, Sanyo uses a liquid-phase epitaxial process to grow the n- and p-type wafers on an n-type substrate. This process is the key to the 0.23% efficient LEDs, which measure 0.3 mm square and yield 7,000 to 10,000 per wafer.

To double the brightness of the display, the assembly on which the LEDs are mounted has a reflective glass sheet. In the sheet are holes to accommodate the 38,400 diodes, and to maximize reflection of light the walls of each of the holes are covered

with a film of thin gold.

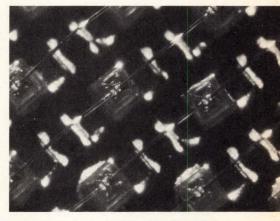
To mate wafers and assembly, Sanyo uses automated die bonding. The assembly is mounted on a table with precisely controllable X and Y motions, and the wafer is placed in a cylinder or collet.

The collet descends toward the table, tests each LED, and a needle in its middle punches out good ones and secures them to the holes in the assembly. The table moves, and the procedure repeats until all the LEDs are installed in a zigzag matrix, with

Thin is in. Flat TV screen, measuring 6.4 by 4.8 inches and 80 mils thick, has fairly good resolution. Green-hued LEDs making up the screen are wire-bonded to an aluminum substrate in a zigzag fashion, top. Screen dissipates 12 watts.

160 diodes per row. The final step wire bonds the top electrodes, using 40-micrometer gold wire.

The TV set has two basic units: the display, housed in a box 460 mm wide by 320 mm high by 80 mm





Electronics review

Researching a flat world

Sanyo's flat-panel TV set with 38,400 light-emitting diodes is not the company's first. Previous versions were a 6,144-LED set [*Electronics*, May 11, 1978, p. 72] and a 17,920-element set described at last October's Biennial Display Research Conference in Cherry Hill, N. J.

Nor will work stop here, says designer Tatsuhiko Niina. He hopes to improve picture quality by adding red, orange, and yellow LEDs; to reduce size and power consumption with custom integrated circuits; and to cut costs by improving the fabrication technique even more. Moreover, LEDs are but one class of devices vying for a share of the flat-TV future. Liquid crystals are under investigation by Hitachi Ltd. [Electronics, May 26, 1977, p. 41] and PanelVision Inc. of the U. S. [Electronics, Nov. 9, 1978, p. 34]. Japan's public service broadcasting system, NHK, is examining plasma displays [Electronics, June 22, 1978, p. 63], and the Hirst Research Laboratories of General Electric Co. Ltd. is studying dc electroluminescents [Electronics, Sept. 14, 1978, p. 63]. Moreover, a Swiss lab has demonstrated the feasibility of a flat CRT [Electronics, July 20, 1978, p. 68].

thick; and the power supply and signal-processing circuitry, which is made up of general-purpose bipolar and complementary metal oxide semiconductors.

The circuits convert incoming analog signals to digital signals that are held in a memory for two horizontal scanning periods. To improve resolution, each line of the signal is duplicated, so that it appears on two different LED rows.

The display has a brightness of 40 foot lamberts at a drive current of 0.5 milliampere per diode and consumes only 12 watts, less than a CRT of comparable size. It can be hung on a wall separate from the power supply and processing circuitry.

Microprocessors

Development station runs eight emulators

Last year, Futuredata Computer Corp., Los Angeles, made news when it lowered the per-station cost of its microprocessor development system by allowing eight designers to share a floppy-disk memory and printer. Carrying the sharing idea further, Futuredata hopes to introduce in July a system that lets each development station handle multiple prototypes—perhaps as many as eight—via slaved in-circuit emula-

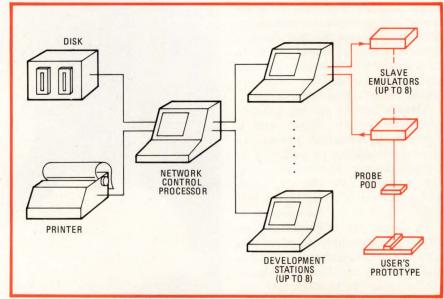
tors. A full-blown system, then, could have as many as 8 master development stations with 8 slaves apiece. Price with 64 prototyping stations: as low as \$6,000 per station.

Inside out. Futuredata can join so many emulators because it brings them outside the development station. Instead of having an emulator dedicated to a station, it loops several of them together via a high-speed serial loop. Thus, one station can control many prototypes. And the microprocessors being emulated can be 8- or 16-bit types from a variety of manufacturers.

According to Futuredata, the prototypes will run at top speed without having to halt, as other systems do, during debug operations while test information is displayed on a cathode-ray tube. "There are other master-slave systems but their processors share a common memory," explains David Ulmer, Futuredata's director of engineering. "When the master is running, the slave can't, and vice versa. We don't do it that way. We can have both executing simultaneously so that we don't have to halt for debug."

In the new Futuredata system, each slave-emulator box has a random-access memory containing software personalized for the processor under test. At power-up, debug routines are down-loaded into the slave's memory. In its earlier design [Electronics, August 17, 1978, p. 89], the memory and "personality" board for the device to be emulated were both in the master station.

Futuredata is still ironing out the final design particulars, one of which is how many slaves to put in the high-speed loop. "The hardware doesn't dictate the maximum," says Ulmer. "We daisy-chain the slaves: the serial line goes into one emulator, then comes out to go to the next. Since you can do this indefinitely, it's really up to the software. My



Multiple stations. As many as eight master development stations can have up to eight emulators apiece in new system from Futuredata that could be out as early as July.

guess is that we'll limit the number to around eight."

Ulmer expects the emulator's memory to be more than capable of handling an 8-megahertz 8086, one of the fastest microprocessors. "That requires a 185-nanosecond device, and we'll probably use 100-ns RAMs," he says. The size of a slave's address space will be 16 megabytes (the amount Motorola's 68000 will access directly). Yet Ulmer predicts Futuredata won't install more than one megabyte because "even that requires 64-K RAMs and we really don't have any yet," he says. "You would need 256-K parts to really do it right." Futuredata has not decided on the exact order of the devices it will emulate, but the 8086 will probably be the —John G. Posa first.

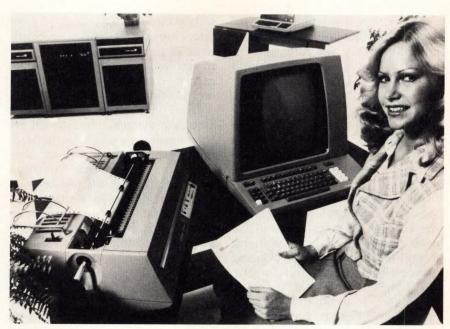
Computers

Business systems doing double duty

It's no longer a matter of either/or, say manufacturers of microprocessor-based small business systems. Rather than specializing in either word or data processing, they must offer both in a package.

Sophisticated and cost-conscious users now balk at buying separate terminals for word and data processing, said marketers showing their wares at Interface 79, the data communications show held earlier this month in Chicago. So they must offer two functions for the price of one piece of hardware to maintain the 35% or better annual sales growth they have been experiencing.

Additions. Manufacturers are adding new software to upgrade existing equipment into combined distributed data- and word-processing centers and to prevent competitors—especially larger equipment suppliers like IBM, Xerox, and Burroughs—from siphoning new business from their old customers. Thus they hope to be on top of the explosive growth expected in the market for small business systems: 1982 sales are



Added capability. Basic Four Corp., Tustin, Calif., shows off its model 730 small-business computer system, to which it has added distributed data- and word-processing modes.

pegged at \$3.55 billion, up from an anticipated \$885 million this year.

Several makers showed their repackaged combination systems at Interface. Others are expected to unveil their offerings later this year.

Basic Four Corp., Tustin, Calif., a subsidiary of Management Assistance Inc., showed its existing 410, 200, and 730 systems in a distributed data- and word-processing mode. The 730, the largest unit with 256 kilobytes of memory and 300 megabytes of disk storage, acts as a message center and periodically polls other network nodes to distribute interoffice mail, orders, and bills. "We're the only vendor offering this kind of thing," claims David Seigle, vice president and general manager of the Distributed Data Processing division.

"With the recent introduction of the DataWord word-processing system, we achieved simultaneous data processing and word processing on the same system," he says, adding that the combination has now been integrated with a distributed network capability. A full-capability system in minimum configuration probably will cost about \$150,000.

Mohawk Data Sciences Corp., Parsippany, N. J., says its combination offering is a less expensive alternative to new competing products. It added word-processing software to its Series 21 models designed for distributed data processing and sells it for \$17,000 per node, including a printer. Comparable competitive systems would cost triple that amount, claims Douglas Davidson, senior vice president for marketing. However, the system is restricted to four keyboards per processor, 64 to 96 kilobytes of main memory, and 1 megabyte of disk storage.

Davidson says the new sophistication of buyers unwilling to duplicate hardware is leading vendors to integrate communications links into the word-plus-data-processing packages. "The key element is now communications. Some customers are already asking for electronic mail."

Others. Although Megadata Corp., Bohemia, N. Y., scheduled a press conference to introduce its series 2001 distributed word-processing system, last-minute delays with software forced cancellation. A model on the exhibit floor had 64 kilobytes of random-access memory and dual disk drives storing 500,000 bytes. Company sources say a distributed data-processing package will be demonstrated this year.

To keep up with the competition, Datapoint Corp., Dallas, will soon

Electronics review

announce a software upgrading of certain distributed data-processing products so they can perform word processing, sources say. Demonstration systems at Citibank and Texaco already are on line.

The next innovation will be downline loading. Instead of isolating the new systems, Basic Four will soon offer a program linking large mainframe processors with its dedicated networks, much like a present feature of Mohawk's systems.

Such announcements make real the concept of merging word and data processing. But as Frederick Wang, director of market planning and development at Wang Laboratories, Lowell, Mass., notes, [Electronics, March 1, p. 14] a lot of user education will be necessary in order to make effective use of the new systems.

-Larry Marion.

Business

U. S., Israel broaden electronic ties

Israel's expanding electronics industry hopes to benefit substantially from the peace treaty with Egypt. The treaty has led to an American decision to allow Israeli firms to compete with American firms for Pentagon contracts. A memorandum of agreement on the subject was completed on March 26 between Secretary of Defense Harold Brown and Israel's Defense Minister Ezer Weizmann and could mean millions of dollars to Israel's defense-related electronics industry.

In the past, very few Israeli electronics firms were able to sell to the Pentagon because of "Buy American" rules, which require foreign bidders to be 50% below American firms in order to be considered. Under the new agreement the American market will be opened up to what one Israeli defense official terms competition on an equal footing with American firms for the whole gamut of sophisticated military electronics gear. He points out Israel's advantage of a large techni-

cally skilled and well-educated labor force working at wages only half those in Europe and the U. S. Electronics production, most of it for export, is valued by the Israelis at over a billion dollars last year.

Israel military electronics and aerospace manufacturers should get before summer's end a list of U.S. military hardware for which they may compete with their American counterparts. The lists will begin to be drawn up during a meeting of U.S. and Israeli defense representatives scheduled to start within 60 to 90 days, according to a Pentagon spokesman.

The agreement also calls for more mutual cooperation between the two countries in research and development, including exchanges of engineers and scientists, and increased procurement and logistics support. The rationale for the agreement, the Pentagon says, is to help offset Israel's negative military trade balance with the U.S. resulting from large purchases of American weapons. However, the memorandum sets no specific dollar value on U.S. military hardware that Israel may supply.

Joint ventures. Director of the Israel Investment Authority, Rafael Benvenisti says he expects the agreement to lead to the establishment of many new joint ventures between American and Israeli electronics firms. In the past, the Pentagon forbade a number of American electronics firms to open plants in Israel because of the sophisticated nature of their technology, he says. "We are now in the process of renewing contacts with three American electronics firms affected by this ban," Benvenisti says, although he declines to name them.

The Aerospace Industries Association of America sees no significant problems with the agreement, according to one official, since many of its airframe and avionics manufacturers already have working agreements with counterparts in Israel. But the Electronic Industries Association says its Government division is still studying the agreement.

-Neal Sandler, Jerusalem

Audio

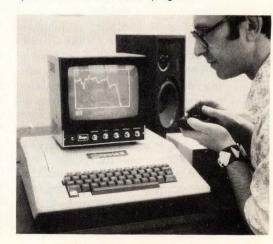
Apple computer checks speakers

Loudspeaker tests are normally done in anechoic chambers so that reflected sound cannot skew measurements of amplitude versus frequency. However, listeners use their speakers not in anechoic chambers, but in living rooms. Since the environments are very different, speaker performance may seem to suffer.

Robert A. Berkovitz, 52, research director of Teledyne-Acoustic Research Inc., Norwood, Mass., one of the country's largest makers of speakers, and consultant David McIntosh, 35, have come up with a portable, microprocessor-based system that can be used to test speakers almost anywhere.

Based on the Apple II microcomputer (from Apple Microcomputer Co., Cupertino, Calif.) with a custom software package and input/output, the system makes possible measurements that are about as accurate as those using anechoic chambers—but without the cost of the chamber, and at a lower hardware cost than competing testers. According to Berkovitz, spectrum analyzers that could do the job cost at least \$10,000 versus the approximately \$1,600 price of the Apple II

Responding. Nine-inch monitor of Apple II computer displays frequency response of speaker determined with FFT program.



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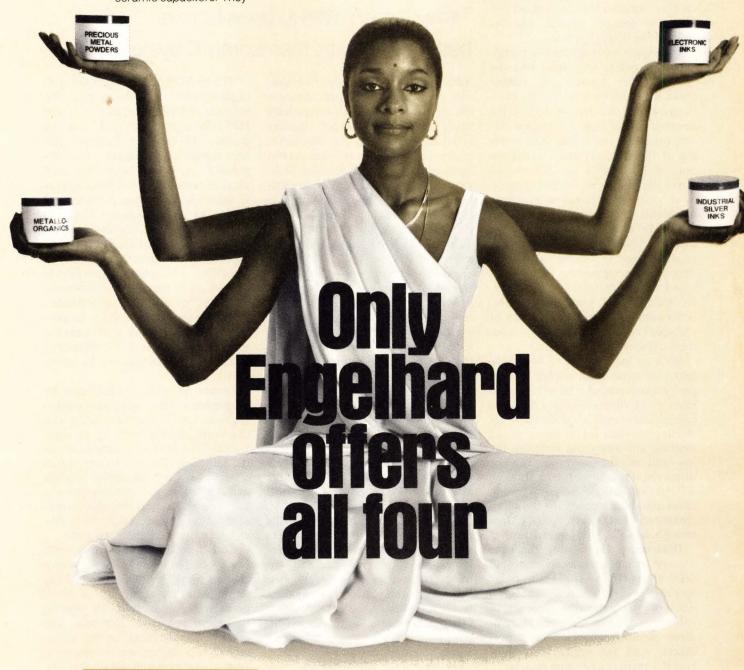
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system with its peripheral attachments for the job.

In action. The system uses a series of 10-microsecond pulses that contain energy of all frequencies, like white noise. These pulses are fed into the speaker terminals, converted to acoustic energy, and received by a calibrated microphone. In effect, the microphone output is an electrical analog of the acoustic output of the speaker augmented by reflections from the speaker cabinet and the walls of the listening room.

The Apple system actually pumps about 16 pulses at a time into the speaker. The Apple's I/O system opens gates, or time windows, so as to catch only the desired part of the acoustic output from the speaker. By electronically controlling the opening of the windows and their duration, it is possible to look at the direct sound coming from the speaker or to include cabinet or listening-room wall reflections.

The 16 acoustic bursts are digitized and summed; this culls out random noise in the test area. The data then is treated to a software-based 256-point fast-Fourier analysis which takes about 3 seconds. Afterward, the spectral response of the speaker is displayed on a video terminal driven by the Apple.

With its sample rate of 46.5 kilohertz, the system can display speaker performance across a band from 200 hertz to 23 kilohertz with a dynamic (amplitude) range of 32 decibels. By shifting the data into a memory and filtering and analyzing it again, the low end of the spectrum can be displayed down to about 25 Hz with 2.2 Hz resolution. The processing takes about 25 seconds for the small computer, but that's plenty fast enough, according to Berkovitz.

Differences. By moving the time window around, engineers can spot differences in a speaker's pulse response at different frequencies. They can also spot the presence of cabinet reflections that might reinforce some frequencies or cancel others. And the system can show how the speaker and room interact.

Acoustic Research engineers are using the setup to help them design

speakers by taking test speakers to actual living rooms and getting a cross section of speaker responses in different environments. The company is also using three other systems it has built as marketing tools. Salesmen use them to demonstrate the basics of a speaker system.

The system has also spawned interest among makers of audio test gear. Although no product developments have yet been agreed upon, it seems fairly certain that low-cost, microprocessor-based spectrum analyzers are on the way, according to Berkovitz.

-James B. Brinton

Navigation

Time-domain filtering gives Lonars better position fix than Loran-C systems

Adding new technology to tried-and-true principles sometimes advances the state of the art with a relatively small investment. Johns Hopkins University's Applied Physics Laboratory has demonstrated that maxim by using time-domain filtering techniques implemented with a Hewlett-Packard minicomputer to eliminate the noise limitations of the Loran-C long range navigation system.

With a Navy investment of approximately \$1 million and two years of engineering effort, the Laurel, Md., lab has come up with a new Loran navigation receiving system called Lonars that can generate a position-fix to within less than 100 feet in real time, five times better than Loran-C [Electronics, March 29, p. 57]. Lonars' developers believe it has potential for navigation accuracies of within 30 feet.

Classified. The Navy, whose Strategic Systems Project office is sponsoring Lonars, already has three prototypes operational, says APL's project supervisor William J. Peters III. Neither Peters nor the Navy will discuss the classified applications, but other sources suspect one of the program's goals is to deploy Lonars aboard the underwater missilelaunching submarine fleet to enhance the accuracy of the Polaris, Poseidon, and upcoming Trident intercontinental nuclear missiles. "Before you can figure out where you want to go, you must know where you are," explains one source. "The more precisely you know your position at launch time, the better your aim."

"Time-domain filtering is the guts of the system," says Peters, since the software technique used in Lonars' HP 2109 mini tracks and edits the pulsed, 100-kilohertz Loran-C station signals to eliminate and compensate for noise. Noise has long plagued users of signals from Loran-C transmitters, whose positions are known to the navigators that use signals from three stations to compute their own position. Whether the superimposed noise originates in lightning or other atmospheric sources or in cross-rate interference generated by a second transmitter's pulse, the result is the same: inaccuracy in measuring the signal's arrival time that produces a corresponding inaccuracy in computing the user's location.

Lonars not only is unaffected by atmospheric noise, says APL project engineer Leo F. Fehlner, but it also can track signals from up to eight Loran-C transmitters simultaneously. Although Lonars uses only three stations for a fix, the ability to track and use additional stations permits the system "to coast through periods of cross-rate interference" from other Loran signals, Peters explains.

Costs. Precision navigation with Lonars could be important for future civilian uses, Peters believes, citing its potential for accuracies of 50 or perhaps 30 feet as useful for piloting in harbors, narrow channels, and other restricted areas, as well as for offshore oil- and mineral-exploration vessels and research ships. But the APL supervisor is quick to add that costs will have to come down

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substantially from the estimated \$80,000-per-system price of the Navy prototypes. Nevertheless, Peters says that the laboratory has already received inquiries from several manufacturers.

As for the HP 2109, Peters says its high speed and 32,000 words of core memory are more than adequate for the application, but the printed-circuit boards are being retrofitted with connectors of military standard. "Its speed is perfect, since it takes only 75 nanoseconds for add or subtract functions and something like 225 nanoseconds to multiply or divide," he says. "The memory is more than adequate. Lonars only requires about 18 to 20 thousand words-about 60% of what is available to us." -Ray Connolly

Medical

Microwaves affect action of Librium

It's close quarters aboard naval vessels and their innards are filled with all kinds of low-level microwave radiation from the ships' electronic systems. There is little or no evidence that the microwave levels affect human biology, so, the reasoning goes, if exposure standards are followed there is no cause for concern.

Or is there? A team of researchers at the Naval Medical Research Institute in Bethesda, Md., has found that low-level microwaves change the way laboratory rats respond to the tranquilizing drug Librium. The radiation has no other apparent effects.

Now a lot of work must still be done before it can be shown that human beings taking Librium would also be affected. But Librium is commonly prescribed to relieve the tensions of shipboard duty, hence the Navy's interest.

The rats worked harder when exposed to as little as 1 milliwatt per square centimeter of pulsed power, according to John R. Thomas, who worked on the project with Linda S.

Burch and Stephen S. Yeandle. This power level, at 2.45 gigahertz, is typical of what is found near radar equipment aboard ships.

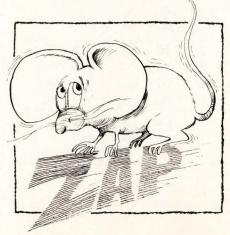
In the tests, the researchers first trained the rats to do certain tasks after giving them Librium. The animals were, for example, taught to push a certain button to reward themselves with a food pellet. This learned, the researchers turned on the microwaves. They observed, simply, that the rats went about obtaining the pellets at a faster rate.

Testing. The microwaves came from a standard-gain horn antenna oriented so the electric field was vertically polarized at the animal's location. Near-field conditions applied since the animals were kept 3.75 wavelengths from the antenna. The average power density was measured with a conventional broadband radiation monitor.

The researchers structured the tests so that the behavior of the rats depended only on whether the microwave radiation was turned on. Extreme care was taken to ensure that behavioral changes were not caused by other variables.

Why the microwaves and the Librium interact is unknown. The researchers have measured rat temperatures and are fairly certain the change in behavior was not due to any heating effects.

In the future, they plan to work with other major drugs that affect the central nervous system to see if their action is also affected by microwaves, according to Thomas, an experimental psychologist. The overall objective, he notes, is to "de-



termine safe [radiation] exposure guidelines." Thomas believes it cannot be emphasized enough that the results of his experiments cannot yet be applied to human beings.

He also points out the big difference between exposing a biological system and the amount of radiation the system actually absorbs. Also important is where the absorption takes place. "Until all research uses the absorbed dose as a common measure, it is very difficult to talk about low-level microwave effects in a general way." -Harvey J. Hindin

Microwaves

NBS builds simple near-field instrument

The electromagnetic radiation emitted by industrial machinery is causing concern among Government health organizations, industries, and also Congress, which is considering legislation to set maximum standards for these emissions. If such limits are imposed, compliance with them will require easy-to-build instruments capable of quick and accurate readings within one wavelength from the source. The National Bureau of Standards, Boulder, Colo., has come up with a prototype of such a near-field device.

"A small, efficient, and accurate near-field instrument would be very welcome," says Mays Swicord, chief of the electromagnetics branch at the Bureau of Radiological Health, Rockville, Md. His branch has been testing industrial machinery—mainly radio-frequency "sealers" used to join plastic sheets together—but to do so is using sophisticated instruments that require considerable skill to set up and interpret.

Lack of tools. "Sixty per cent of the radiation problems are in the near field yet there is a lack of tools for really getting a handle on measurements in that region," says Charles K. S. Miller, chief of the electromagnetic-interference radiation hazards metrology program responsible for the prototype. Com-

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Electronics review

News briefs

Chips cut Dataspeed's lease costs

Microprocessors make for lowered prices in the American Telephone and Telegraph Co.'s new Dataspeed 4540 clustered-terminal system. The system adds a new cluster controller and individual display controllers to the Dataspeed 40/4 line. The cluster controller uses a Z-80 8-bit microprocessor to interconnect as many as 24 displays and eight printers. Underneath each display is a controller with its own Z80 and a video controller chip developed by subsidiary Teletype Corp. A typical system with three displays and an 80-column printer should lease for \$600 to \$700, depending on options. A similar system from IBM leases for slightly over \$900.

PAVE PAWS radar in final tests

The U. S. Air Force's Sixth Missile Squadron is putting the controversial PAVE PAWS missile-warning radar through its final tests, following USAF acceptance earlier this month of the Cape Cod, Mass., phased-array system from prime contractor Raytheon Corp. A final environmental impact statement on the massive radar [*Electronics*, Dec. 7, 1978, p. 8] will be published in May, and the Air Force hopes to declare it operational in June.

Apple to bite into educational market

Apple Computer Inc., Cupertino, Calif., will take its personal computers into the educational market in a contract with Bell & Howell Co., Chicago. The move gives Bell a new medium for its educational materials libraries and offers Apple ready resources for software packages, as well as access to an education-oriented distribution and repair network through Bell's 100 audiovisual equipment centers.

National to produce PAL chips

National Semiconductor Corp. has signed a world-wide, nonexclusive agreement to produce all 15 of Monolithic Memory Inc.'s programmable array logic chips. MMI, in Sunnyvale, Calif., will supply the Santa Clara firm with all the PAL mask sets, circuit diagrams, and technical information needed to produce the bipolar fusable-link devices. These bipolar replacements for random logic are popular with makers of small computers. A year ago, MMI signed a similar agreement with Raytheon Co.

Hitachi to second-source 68000

With first chips of its MC68000 microprocessor expected in mid-May, Motorola's Integrated Circuit operation in Austin, Texas, has confirmed reports that Hitachi Ltd. will second-source the 16-bit machine [Electronics, March 29, p. 36]. Sources say the deal calls for Motorola to provide the Japanese firm with tooling for production of a mask-compatible alternative. Already a second source on the 8-bit MC6800, Hitachi will also be given rights to, and help develop, 68000 peripherals. There is still no word on a U.S. second source for the 68000, which will compete with the emerging 16-bit processors from other makers, all of whom have signed second sources.

mercial probes are available, such as Narda's model 8600, but Miller says none offers the same combination of frequency range, sensitivity range, and isotropic characteristics (independence of position in the field) as the NBS prototype, or emi probe, as it is called.

Wide range. The prototype is designed to operate over the broad frequency range of 500 kilohertz to 1 gigahertz, according to Miller's de-

puty, Francis X. Ries. Its wide dynamic range of 1 volt per meter to 1,000 v/m, or 30 decibels, covers the spectrum of field strengths likely to be emitted by high- or low-level sources, he says.

The probe is in two sections—a box containing the electronics and a hand-held antenna designed to be isotropic. Instead of one dipole, there are three for detecting simultaneously three orthogonal electric-field

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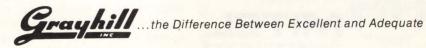
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Electronics review

components. The dipoles are electrically short and each has a beam-lead diode ultrasonically bonded to its junction. Short dipoles, however, are high Q circuits and therefore have a narrow frequency response.

To broaden the response, the circuit's equivalent resistance must be made higher. The designers do this by using highly resistive leads (80 kilohms per centimeter) made from Teflon impregnated with carbon and extending the full length from the dipoles to the opposite end of the 1-meter-long handle that supports them. Low-resistance cables carry the signals from this end of the hand-held wand to the boxed electronics where they are converted into individual readings or a vector-summation reading of all three.

Easy to build. Sensitive to criticism that NBS designs are often extremely expensive to build, Ries says the designers took special pains to make the probe easy to manufacture. Off-the-shelf parts are used wherever possible, he says.

Also, the prototype is not meant to be an exact model. "There's plenty of room for shrinking the size of the box—now 17 cm high, 21 cm wide, and 20 cm deep—and the boards," Ries continues. NBS plans to make several prototypes that it will give to selected manufacturers for examination to determine their interest. Ries estimates that a mass-produced version could be made to sell for roughly \$3,000.

-Robert Brownstein

Weather

\$10,000 station sends to satellite

Anyone unfamiliar with satellite earth stations priced in the \$10,000 range that can be put together in three hours probably has not heard of Electronic Techniques Inc. Yet the little Fort Collins, Colo., company has made itself known to the Department of the Interior, which has awarded it a \$1.5 million contract to build 150 portable, solar-powered earth stations over the

period of the next 20 months.

Interior's Bureau of Reclamation says it plans to use the stations in a meteorological surface observation network, called Mesonet, to relay data hourly via NASA's geostationary operational environmental satellite (GOES) to ground stations. From there the data is to be relayed to a computer complex at Reclamation's Engineering and Research Center at Denver.

Using lead-calcium batteries from Delco Electronics and drawing power from Arco Solar silicon photovoltaic solar cells, each Mesonet station's sensors will measure the usual remote weather station parameters—wind speed and direction, temperature, humidity, barometric pressure, precipitation, and battery status. This will be done at 5-minute intervals for hourly digital radio transmission to the satellite. Signals are sent via a Yagi antenna in the 402-megahertz region assigned to the GOES satellite.

What is remarkable about the Mesonet stations, according to Interior officials, is their high reliability and relatively low cost. Even in the unlikely event the solar panels receive no sun for 30 days, for example, the batteries can still continue station operation. The stations, aluminum rods shaped into triangles and standing 20 feet tall, are designed to withstand winds in excess of 100 miles per hour. The weather sensors and electronic equipment will all be off the shelf.

Big money. The \$1.5 million competitive award represents big money for four-year-old Electronic Techniques, says vice president Vincent Scheetz. The privately held company's annual volume last year was about \$1 million.

Interior says the Mesonet stations will be used to advance the agency's investigations of cloud seeding and natural irrigation created by runoff from mountain snowpacks. The initial 25 stations will be deployed in an area with a radius of 150 kilometers near Big Springs, Texas, Scheetz says, while others will be used later at research sites in Montana and elsewhere.

-Ray Connolly

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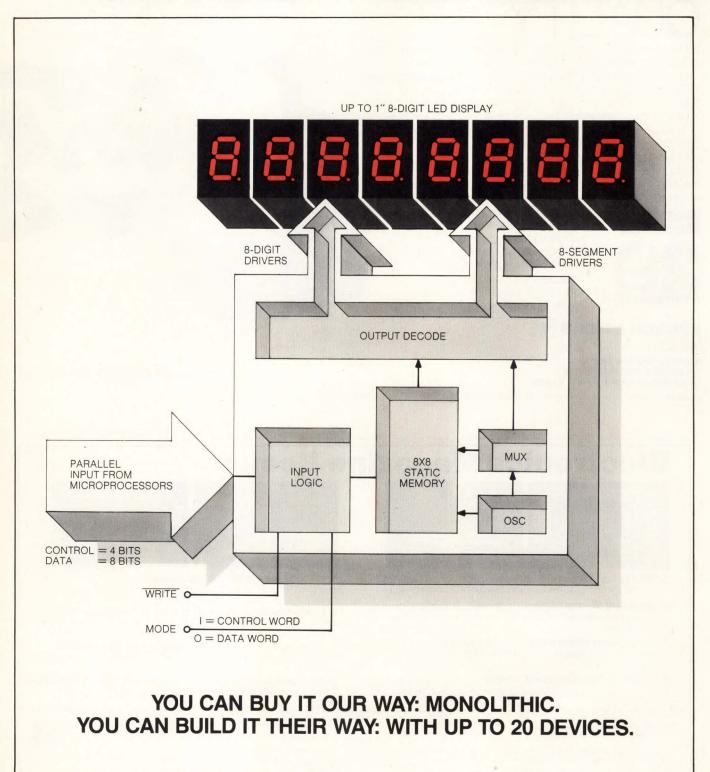
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Washington newsletter.

FCC urged to act on opening Japan's data market

Pressure is being put on the Federal Communications Commission to deny applications of three American-based international record carriers to provide their data services between Japan and the U.S. until their Japanese counterpart, Kokusai Denshin Denwa Co., opens its domestic data-distribution system to competition. Petitions to deny the applications of ITT World Communications, RCA Global Communications, and Western Union International to work with KDD were filed in mid-April by the Association of Data Processing Service Organizations (Adapso), the Computer and Business Equipment Manufacturers Association (CBEMA), and Control Data Corp., whose Japanese data-processing subsidiary is limited to communicating with a single U.S. computer center via a leased line. KDD controls and restricts the use of private-line circuits in Japan.

The three opponents of the application contend that the restrictions are inconsistent with the recommendations of the CCITT, the international record-carrier organization. If the FCC does not issue a denial aimed at opening the Japanese market, Adapso says, the commission should investigate "KDD's actions in restricting private-line service and requiring the use" of its specialized data services in Japan by U. S. carriers.

China wants Westar for domsat, U. S. confirms . . .

China has decided what it wants in a domestic satellite system. It would have 12 C-band transponders with time-division multiple access like the Hughes Aircraft Co.'s Westar built for Western Union, say State Department officials, confirming an initial report last year [Electronics, Oct. 26, 1978, p. 57]. However, the Chinese are still undecided on selection of ground stations, despite reports that Hughes is offering them a complete package of ground stations to use with satellites that would be launched by the National Aeronautics and Space Administration.

. . as Westar extends Mailgram coverage to Southeast

Western Union Telegraph Co., meanwhile, is touting its operating Westar satellite and ground stations equipped with time-division multiple access as its "electronic mail system of the future," using a 16-foot antenna prototype at its Miami, Fla., offices to demonstrate Mailgram message transmissions from its earth station outside Atlanta. Western Union says the earth station will be permanently connected to the Miami post office late this summer, with other earth stations to be added later this year at Tampa and Orlando, Fla.; Memphis, Tenn.; and Charlotte, N. C.

U. S. suppliers told to work harder for NATO business

American military electronics contractors must be better represented and more competitive at North Atlantic Treaty Organization headquarters in Brussels if they expect to get some of the \$1.2 billion worth of command, control, and communications hardware business the alliance expects to do during the next five years. According to T. Joseph Loveland, director of the U. S. NATO mission's infrastructure division, approximately \$400 million will be spent for tactical point-to-point and mobile communications systems, with an equal amount available to enhance the NATO air defense ground environment, known as Nadge. Another \$300 million to \$400 million will go for outlays on such basic electronics as radars and fixed communications systems.

'April 26, 1979

Washington commentary

Solar-power satellites in a time of timidity

Whatever became of the Flippo bill? H. R. 2335, last year's proposal by Alabama Democrat Ronnie Flippo to spend \$25 million on the evaluation and demonstration of a solar-power satellite (SPS) is still resting in a House subcommittee [Electronics, April 27, 1978, p. 60]. On the Senate side, no counterpart to it even exists for examining space-based systems that would convert the sun's energy into electricity and transmit it as microwave power to antennas located on the earth.

The Solar Power Satellite Research, Development, and Evaluation Program Act of 1979 has been modified to eliminate a single, large-scale demonstration program and confine expenditures largely to earthbound tests and paper studies of the SPS system's technology and its societal impact. This has gained it more sponsors. Yet diminished opposition hardly guarantees success. Even with passage in both the House and Senate, the effort is likely to produce no more than several stacks of interesting and sometimes conflicting studies that will never come to the attention of the one person who could bring them to life, the President.

Commitment from Carter

Jimmy Carter might consider adapting a page from John F. Kennedy's special second State of the Union message in 1961. This year marks the 10th anniversary of America's successful manned lunar landing, a program to which President Kennedy committed himself in May 1961. Its cost was enormous, and so was the controversy that surrounded it-yet what Kennedy called "this great new American enterprise" served to restore a declining American world image, spark the national imagination and the economy, significantly advance technology, and make space a place "not filled with weapons of mass destruction, but with instruments of knowledge and understanding for the progress of all people."

Two other aspects of SPS are equally important. A national commitment to such satellites by the President would serve notice on the cartel of oil-exporting nations known as OPEC that the Western world can tolerate no longer the economic blackmail their price-fixing represents. Moreover, by making participants of other nations, some of which have already expressed interest in the concept, the President could take a long step toward improving America's strained relations with these allies.

The technological and societal challenges of

SPS are admittedly enormous. Solar power has a soothing sound in contemporary jargon, but microwaves rate as high as nuclear radiation in any lexicon of scary sounds. As one reader put it a year ago, solar-power satellite stories should be headlined "How to fry New York in 2½ hours." The comment is still more evidence of a national malaise that Arthur Kantrowitz labels the time of timidity.

"The time of timidity is best defined by contrast with the idea of progress," explains Kantrowitz, who directs the Avco-Everett Research Laboratory. "Progress, to my mind, is best described by the distinguished philosopher of science, Sir Karl Popper's description of the scientific method; namely, it is trial and elimination of error. By contrast, in the time of timidity, we eliminate errors first. Before we act, we will insist on a certainty human beings can never attain."

Action or reaction?

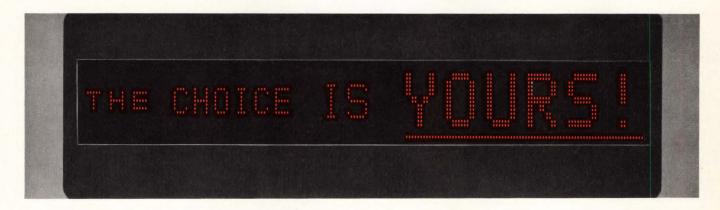
For America's timid leaders in the White House and the Congress, where reaction to potential disasters has taken precedence over positive, imaginative action, Kantrowitz has two caveats: "First, that perhaps the time of timidity might not be all-inclusive. Unless the idea of progress can be stamped out everywhere, we must expect that technological surprise might still intrude from those barbarian domains where the idea still survives.

"The second caveat is that, in the nearly stagnant society, any residual action may result in irreversible side effects—whereas in a time of technological progress, unanticipated side effects, which do not appear until years later, can be more readily dealt with by a technology which will have greatly advanced in the meanwhile. Thus, there are important forces that drive the nearly stagnant society toward complete stagnation, or more hopefully toward a renewal of vigorous technological progress."

Much of the technology for making a vigorous start on SPS is already in place. Still, much research and development remains to be done, and it must be done carefully, particularly in such areas as the impact of microwave transmissions on the ionosphere. But those efforts deserve to be accelerated far beyond anything that can be accomplished by Ronnie Flippo's proposed outlay of \$25 million—an amount that today will barely pay for one new fighter plane, let alone the jet fuel and lubricants required to fly it.

Ray Connolly

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NEC Newscope

ND-10 Large-Capacity ESS Lauded By

Tennessee Firm

Telephone and Data System, Inc. (TDS) in Concord, Tennessee reports its NEC-built, large-capacity electronic switching system is performing beautifully.

The system, an ND-10 stored program controled ESS, was officially cutover at Concord last October. It provides 8,000 lines to serve the people of Concord, a community that is growing rapidly in population. It is the first building-type ND-10 system ever commissioned in the United States.

The Concord system offers such custom call features as call forwarding, call waiting and abbreviated dialing. In addition, it is equipped with the LAMA (Local Automatic Message Accounting) feature, which allows the company to ticket its own direct distance dialing traffic.

Mr. LeRoy T. Carlson, Jr., TDS's Executive Vice President, said that his company has received many calls from customers who are very pleased with the services provided by the ND-10 system. Mr. Carlson, Jr. also said, "It is a truly outstanding switching machine and we believe the best in the world."

The system is interfaced with NEC's Technical Assistance Service Center in



Mr. Fred T. McPhee (left), President, and Mr. R.C. Eldridge, General Manager, Concord Exchange, Inc., look over ND-10 ESS.

Dallas, Texas, so that it can benefit from remote maintenance services.

The ND-10 is one of the most advanced fully stored program controled ESSs manufactured by NEC.

Designed for medium to large line capacity of up to 160,000 and equipped for nearly 30 standard service features, it can also have about 30 useful optional service features.

In addition to the Concord system, twelve ND-series electronic switching systems are now in service in the U.S. providing a total of more than 35,000 lines, and another is currently being built.

New FET To Replace TWT

NEC recently announced the successful development of a series of new GaAs power FETs which can replace conventional traveling-wave tubes used in microwave systems.

The new GaAs FETs can deliver an output power of 15W at 6 GHz, 10W at 8 GHz, 2.5W at 11 GHz or 1.1W at 14 GHz.

To obtain high output power with a GaAs FET, it is necessary to optimize the device structure so that the device has a high breakdown voltage, high gain, good matching and reproducible fabrication process. NEC has developed a new FET structure called the "graded recess structure" which meets all of these conditions.

The new FET, no bigger than 1 cm square as against a traveling-wave tube measuring about 30 cm in length, will reduce the size of microwave equipment remarkably. It will also greatly reduce power consumption and increase the reliability of microwave systems.

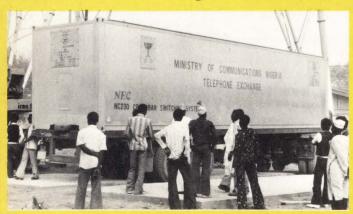
NEC has also completed an amplifier capable of producing 22W in the 6 GHz band, by coupling two new FETs.

ing already been commissioned and the other seven now undergoing acceptance tests. Installation of the remaining 19 systems will be completed toward the end of this year at important cities throughout the country.

These van-type crossbar switching systems will provide a total of 23,400 high-grade telephone lines.

The NC230 is a small-capacity, high-mobility crossbar switching system designed by NEC. It offers a choice between the 500-line and the 2,000-line van or building types. Its capacity can be expanded up to a maximum of 10,000 lines by multi-unit installation. It is flexible enough for use as a local exchange, trunk exchange or can be interconnected with existing switching systems. Simple connection of external cables is practically all that is required for installation, and maintenance is very simple.

Nigeria's Direct Dialing Network Ready This Year



One van-type switching system arrives at installation site.

Nigeria will have its nationwide subscriber direct dialing telephone network completed toward the end of this year.

The Posts and Telecommunications, Nigerian Ministry of Communications is carrying out the project.

NEC has shipped twenty-nine NC230 van-type crossbar switching systems.

Of the 29 systems for the project, six were airlifted from Japan with three hav-

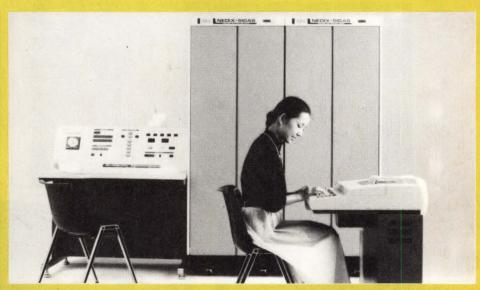
ANTARA Has Installed ESS For National Telex/Data Link

The National News Agency Institute of Indonesia, known as ANTARA News Agency, has installed an advanced electronic telex/data switching system, to link its branch offices throughout the country.

The system, NEC's NEDIX-510AS stored program controled time division electronic telex/data switching system, links 11 branch offices in such important cities as Medan, Bandung, Jogjakarta and Surabaja. It will be expanded to cover 26 branch offices in future.

The system is provided with a special multi-address call service feature so that a telex message can be simultaneously transmitted to all branch offices.

The NEDIX-510AS, capable of accommodating up to 1,920 lines, is a small capacity version of the NEDIX-510A stored program controled time division telex/data switching system with a capacity of up to 30,720 lines. It can be expanded up to the full capacity of the



large model, the NEDIX-510A system, as needs arise.

Since the latest, most sophisticated electronic components are used throughout, the NEDIX-510AS system is extre-

NEDIX-510AS stored program controled time division electronic telex/data switching system

mely compact, highly reliable and economical to operate.



New DME Navigational Aid Already Becoming Popular

NEC-developed all solid-state DME (Distance Measuring Equipment) is becoming popular around the world.

The equipment, the first all solidstate unit ever developed, is offered in two models depending on output power - 100 W and 1 kW - in the NNG-500 series line.

The new DME uses a newly-developed 1.6 kW transistor power amplifier which allows the equipment to cover its working frequency range from 962 MHz to 1,213 MHz with no need for adjustments.

In addition, the new DME incorporates a digital monitoring system and a remote control system using a microprocessor to provide multiplex control

The NNG-570 all solid-state DME measures 1,960 mm (h), 570 (w) and 450 (d) and weighs 260 kg. Each panelled unit is easily accessible for maintenance.

by a single telephone channel, as well as easy maintenance.

NEC has already shipped a 1 kW all solid-state DME to El Salvador for its Cuscatlan International Airport and seven VOR/DME systems using the new DME are now being manufactured for Sudan.





King Carl XVI Gustav of Sweden on the right in these photos—presents the 1978 Nobel Prize in Physics to Bell Laboratories scientists Robert Wilson (top photo) and Arno Penzias.

What does the Nobel Prize have to do with your telephone?

The two scientists on the opposite page are receiving the highest honor a scientist can earn—the Nobel Prize. They are the sixth and seventh laureates who did their prize-winning research at Bell Telephone Laboratories. These scientists shared a common goal—the search for new knowledge to further advance the art of telecommunications.

Clinton Davisson shared the Nobel Prize in 1937 for demonstrating the wave nature of matter. In 1956, John Bardeen, Walter Brattain and William Shockley were honored for their invention of the transistor. Philip Anderson's theoretical work on amorphous materials (such as glass) and on magnetism led to a Nobel Prize in 1977. And in 1978, Arno Penzias and Robert Wilson received the Prize for detecting the faint radiation from the "big bang" explosion that gave birth to the universe some 18 billion years ago.

The search for knowledge

These scientists and their colleagues at Bell Labs, given the freedom to explore, have proved

time and again the value of investment in research—not only for telecommunications but for society in general. The transistor, for example, revolutionized communications and brought into being entire new industries—indeed, a new industrial society—based on solid-state electronics.

Other Bell Labs advances—products of this same research environment—have included high-fidelity recording, sound motion pictures, long-distance television transmission in the United States, the electrical digital computer, information theory, the silicon solar cell, and the laser. The impact of this work—on almost every field of commerce, industry, education and even medicine—has been incalculable.

The innovation process

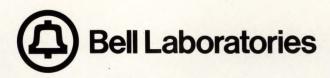
Research done at Bell Labs in the past is the basis for the products and services the Bell System offers its customers today, just as the research going on now is the foundation for tomorrow's telecommunications.

Bell Labs scientists specialists in physics, chemistry, mathematics and many other disciplines—team their efforts with those of our systems, development and design engineers. They, in turn, work closely with Western Electric manufacturing engineers and with the people of the Bell System operating telephone companies.

This technical integration is the foundation for true innovation. One idea feeds another. A basic scientific discovery can make possible entire new technologies and products for telecommunications, and a concept for a new product or system can stimulate the research to find even more new knowledge. That interaction, that teamwork, has been extremely productive: Bell Labs people have received 18,645 patents between our founding in 1925 and the end of 1978.

Sometimes, the search for knowledge may lead to a Nobel Prize. Often, it benefits all of society. And always, its ultimate aim is better service for Bell System customers.

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MWS5101EL-3	200	350	5	0 to +70	2.94
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International newsletter.

Manchester U. develops bit-slice multiplier for super-mini

For its projected MU6-G super-performance minicomputer, Manchester University's computer science department is developing a multiplier unit that gives the product of two 64-bit numbers in 290 ns yet fits onto a single printed-circuit board roughly 16 by 8 in. To meet the twin objectives of high performance and low cost, the group uses a 2-bit-slice multiplier chip with an uncommitted emitter-coupled logic array (ULA) from Plessey Ltd.'s Allen Clark Research Centre in Caswell, Northants. The projected unit comprises 71 ICs—one tenth the number obtained with standard logic—but further process refinements from Plessey will cut the chip count to 56 and the multiplication time to 115 ns. The group has already proved its bit-slice multiplier in a 16-bit version, which uses nine 28-pin ULAs and has a multiplication time of 115 ns.

Sorting system listens to operator to route packages

West Germany's post office research lab in Darmstadt is trying out a computerized package-sorting system that responds to spoken words instead of to the keyboard signals formerly used. The operator pronounces the digits of the postal code on the package into a headset microphone, controlling the system so that the package is routed into its appropriate destination bin. With trained, even-voiced operators, the post office says, the level at which the digits are correctly understood is nearly 100%. The system, which will go into regular service soon, according to officials, can recognize up to 32 words. It features a plausibility check whereby a nonexisting postal code is recognized as such and indicated on a display. British EMI-Threshold Ltd. makes the voice-recognition equipment.

Japanese shrink processor's channel length to 1.5 μ m

As part of Japan's very large-scale integration project, NEC-Toshiba Information Systems Inc. has reduced the linear dimensions of an 8-bit microprocessor 30% to give an area half that of the original chip. Although the work is essentially a straight shrinkage from 4- to 2.8-\mu m design rules, MOS transistor channel lengths are only 1.5 \mu m in finished devices. Overall chip size is only 3.8 by 3.8 mm, with approximately 7,000 gates, or about 480 gates/mm². The devices were fabricated at NEC-Toshiba's Horikawa-cho laboratory, which is in Toshiba Corp.'s works in Kawasaki. Toshiba project engineers say the device uses the instruction set of a common microprocessor—they refused to say which, but a good guess is the 8080A, which Toshiba produces commercially. Toshiba does say that yield on its pilot line has been good, but commercial production is at least a year away.

Pye readies SSB system to cut bandwidth

Prototype 5-kHz vhf single-sideband mobile-radio equipment, capable of doubling and theoretically even quintupling spectrum utilization, is receiving its first public airing in London this week. The system, developed by Pye Telecommunications Ltd. in Cambridge in collaboration with the Philips Research Laboratories, Redhill, uses a pilot carrier at power levels one fourth to one tenth that of speech to provide an automatic gain-control signal needed to overcome vhf fading and to provide a local frequency reference. As a result, claim Pye engineers, fading is eliminated even at speeds up to 70 mph and sensitivity to mistuning is ±150 Hz. This is within the capability of high-stability crystal techniques [Electronics, Sept. 14, 1978, p. 67], one of which can generate all required channel frequencies with a two-chip frequency synthesizer set also developed at the Philips labs [Electronics, Aug. 31, 1978, p. 74].

International newsletter

Fujitsu uses high-density logic to counter IBM

Firing another salvo in answer to IBM's 4300 mainframes, Fujitsu Ltd., Japan's largest computer manufacturer, has started selling four new computers using high-density logic and memory. The M-130F, -140F, -150F, and -160F span the range from somewhat smaller than the IBM 4331 to about 10% larger than the 4341 [Electronics, Feb. 15, p. 85]. The central processing unit of the three smallest models employ newly developed 600-gate master-slice arrays using low-power Schottky technology. All feature 64-K memory chips (for computers delivered after Dec. 1), 1,500-gate n-MOS logic chips in the service processor, and a 6,000-gate complementary-MOS logic chip in the display controller. Minimum rental prices range from about \$5,000 to \$22,500 a month. Fujitsu has also started sales of the Facom V-830, a small computer competitive with IBM's System/34 but incompatible with the M series mainframes. The V-830 contains a 10,000-gate C-MOS processor. Memory is up to 512 kilobytes, and purchase prices start at some \$79,500.

West German firms divide up Awacs contract for NATO

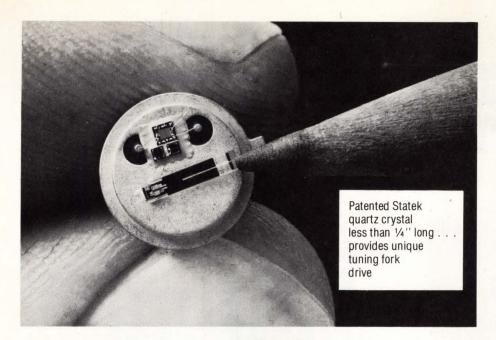
Only a few months after getting the go-ahead from the Bonn government, the major West German companies to work on the Boeing Co.'s E-3A Airborne Warning and Control System, or Awacs [Electronics, Nov. 9, 1978, p. 50], are already lined up for the job of equipping the Boeing 707-320B aircraft with electronics gear. Dornier GmbH has overall responsibility for system integration and installation of the avionics hardware. Other firms participating in the project are AEG-Telefunken, Siemens AG, and Elektronik System Gesellschaft, which will implement the Awacs data-communications system. The first aircraft is scheduled for delivery to North Atlantic Treaty Organization forces by 1982.

France completes initial VLSI phase

The government's drive to make sure France will have a strong IC industry in the era of very large-scale integration is now through its first stage—signing up suitable American partners for the French companies that will share nearly \$150 million in aid over the next five years. The last pairing became official this month when National Semiconductor Corp. and Saint-Gobain Pont à Mousson, a major industrial group, set up Eurotechnique SA. The new company plans to start producing MOS memories and microprocessors by 1981. There are two other MOS makers in the government's scheme: Efcis, a joint venture between Thomson-CSF and Commissariat à l'Energie Atomique (CEA), which is getting its technology from Motorola Semiconductor; and Matra-Harris Semiconductors, which will concentrate on complementary-MOS devices. The bipolar effort is split between the Sescosem division of Thomson-CSF and RTC-La Radiotechnique Compélec, the lead house for emitter-coupled logic in the Philips Gloeilampenfabrieken group.

Addenda

The Canadian government will spend approximately \$161 million (U. S.) over the next three years to help develop products and technologies in the electronics and telecommunications industries. . . . Production of bipolar ICs will begin in July at a pilot plant of Taiwan's Electronics Industry Research Center under a technology-transfer arrangement with RCA Corp. The necessary equipment has been installed, and a group of technicians sent to the U. S. for training last year will be returning shortly.



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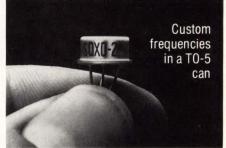
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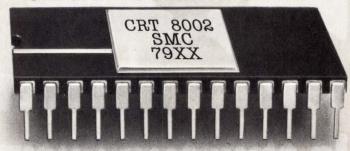
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Significant developments in technology and business

Bonding hybrids to heat sinks cuts weight, volume

by Kevin Smith, London bureau manager

Ferranti technique forgoes printed-circuit boards, reduces cooling requirements by cutting thermal resistance

In the shrinking world of microelectronics, the packaging frequently dwarfs the hybrid or integrated circuitry it contains. But substituting metal heat sinks for printed-circuit cards may offer a way to cut the volume and weight of the package and improve the thermal management of the resulting system.

This technique is under development at the Electronics Systems department of Ferranti Ltd. for high-performance radar systems and other avionics payloads. It could cut the weight of a 300-pound radar by one third, says John Morrison, head of the hybrid microelectronics group at Edinburgh. Such a savings in the avionics payload could lop 200 lb off airframe weight, he notes.

In Ferranti's HELP (hybrid electronic light-weight packaging), as many as four 5/8-inch-square flat packs, each containing a hybrid circuit, are bonded directly to a standard 3-by-2-in, heat sink. Each of these modules is equivalent to a 7-by-4-in. pc board. The technique is compatible with thick- and thin-film hybrids and discrete components.

Savings. As many as 25 HELP modules plus motherboard will fit in a metal case, together with a potted power supply from Power Cube Inc. (see figure). The resulting weight is 4.7 lb, compared with 26 lb for a multiple-board version, and the volume is 124 in.³, versus 926 in.³

Adhesive bonding of the thin-film hybrid packages directly to the heat sink ensures an extremely low thermal resistance relative to the standard method of mounting flat packs on pc boards. Heat sinking cuts the requirement for cooling air flow, allowing a far higher board density to be achieved for the same device junction temperature.

Plug-in. The base of the HELP container holds a multilayer pc motherboard, into which each module plugs by way of an 80-pin edge connector. The leads of the flat packs are inserted directly into the edge connector.

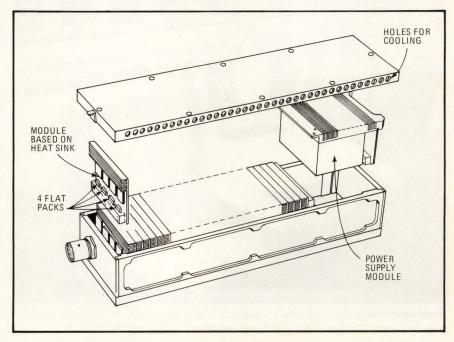
The container fits into a cooling tray with two full-length slots in its

base to permit air to enter. Drilled holes in the container let the air flow across each module. This approach ensures a parallel air flow; the usual approach is to let the air in one end of the unit, which means the cards at the other end might receive a heated air flow.

Cooling can be tailored to the dissipation of each module by blocking the flow across the heat sink's cooling fins. The air flow requirement for identical device temperatures drops from 35 to 15 cubic feet per minute, Morrison says.

The company says the modular approach makes fast turnaround one of the advantages of HELP. A prototype printed-circuit board can be

Shrinking the package. Mounting flat packs containing circuitry onto a heat sink instead of onto printed-circuit boards gives a module with significant size and weight savings, as well as less need for cooling air flow. As many as 25 modules fit into a container.



Electronics international

turned into a thin-film hybrid module in days, Morrison says.

At the moment, the microelectronics group is moving from its first prototype to a radar-scan-converter test unit that will fly in a Harrier jet fighter. After these trials, Ferranti plans to build future-generation radar systems with HELP and to introduce the technology commercially.

Belgium

Personal computer aims at households with extensive hardware, software choices

Europeans shopping for personal computers will get one more choice: Data Applications International (DAI), a small Belgian microcomputer systems house, launches its personal computer at the May 8–10 Compec '79 minicomputer show in Brussels, the firm's home town.

It will join such well-known American brands as Apple Computer Co.'s Apple II, Commodore International Ltd.'s PET, Tandy Corp.'s TRS 80, and MITS Inc.'s Altair—as well as some European machines on the market. But Claude Simpson, managing director, insists the new DAI personal computer will not compound consumers' confusion.

For the home. "This is a secondgeneration personal computer that will sell for under \$1,000," he says. "It is not oriented toward data processing but toward recapturing resources available in households."

One thing is sure: DAI's personal computer will become a familiar object in literally thousands of Dutch households starting this fall. In October, Teleac NV, a nonprofit foundation in Utrecht, will start airing a 20-week-long course on microcomputer programming over the Dutch educational TV network and has settled on DAI's new machine as the hardware.

It has ordered 1,000 of them to resell to its students, who will pay some \$45 for course materials and quiz corrections. The personal computer, an option, costs \$900.

Enrollment. "We had 13,000 students for our first series on hard-

courses. Since a lot of the learners work in groups for their employers, he figures most of the computer buyers at the outset will be companies rather than individuals.

Simpson, of course, is aiming for a much wider market. "Most first-generation personal computers were aimed at professional applications," he explains, "although the Apple II added educational applications. We see other household uses as well—home bookkeeping, health monitor-

ware, and we expect at least 10,000

for the series on software," reports

Chriet Tellulier, Teleac's project

director for the microcomputer

generation personal computers were aimed at professional applications," he explains, "although the Apple II added educational applications. We see other household uses as well—home bookkeeping, health monitoring, and building and garden management. Clubs are another promising outlet." To cover this applications spectrum, DAI designed the microcomputer with a lot of memory, a panoply of input/output possibilities, powerful graphics, and what Simpson calls "graphical sound."

Choices. Thus the 8080A microprocessor around which the machine is built can have anywhere from 4 to 48 kilobytes of random-access memory to work with for program memories. There are sockets for 24 kilobytes of read-only memory, but the system actually uses only up to 22, enough for extensive software like a Basic pseudocode compiler, integral and floating-point math, debugging monitor, and standard 8080 software library packages. There is also a socket for an Advanced Micro Devices 9511 math chip.

As for I/O, the microcomputer has an ASCII keyboard, for starters. Then there are interfaces for a pair of audio cassettes (for low-cost memory storage), game paddles, and serial I/O peripherals meeting the RS-232 standard, plus a modulator that feeds both video and sound into a TV set through its antenna.

Looking outward. As if this were not enough, it is possible to hook into the system bus and through it interface with almost every common electrical control signal through the "real world" cards that DAI makes for automated systems.

In the least expensive versions, the personal computer will have blackand-white graphics that can put



Homeward bound. DAI's personal computer has up to 22 kilobytes of ROM and up to 48 kilobytes of program RAM, together with a range of input/output devices.

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Electronics international

diagrams or 24 lines of 64 characters (or a combination of graphics and text) on a television set. It was designed, though, with color in mind—it can handle up to 16 colors selected through software, with up to 260 lines of picture elements, 352 elements per line. Furthermore, the displays can be moved around easily by programming, through a scheme

developed by DAI that mixes control words and display words.

The new machine also produces audio through a TV or a hi-fi set by means of three oscillators and a white-noise generator. Frequency and amplitude can be programmed over the whole audio range in order to make simple music and gutteral vocal sounds.

-Arthur Erikson

In designing the new LCD, the researchers took advantage of the particular sensitivities of both the nematic and smectic states. The horizontal rows on the display consist of a network of tiny resistances, and the vertical columns are controlled by a network of electrodes. Between the two grids is a thin layer of liquid crystal in the smectic state.

France

LCD uses three molecular states to produce experimental TV picture

The fuzzy gray images on the tiny screen seem incapable of ever rivaling the brightly colored, crystal-sharp pictures on television screens just a few steps away. But scientists at Thomson-CSF's central research labs, Courbeville, believe the projection liquid-crystal display they showed for the first time at the Paris electronic components show in early April could one day replace cathoderay tubes in all sorts of applications.

Three, not one. Their new LCD, they say, has that promise because it exploits the smectic, nematic, and isotropic states of liquid crystals. Previous LCDs have stuck to the nematic state and, though adequate for slow-changing watch and instrument displays, have not been fast enough for video displays.

Thomson's LCD is still very much in the development phase. The device measures just 4 by 5 millimeters and projects an image onto a viewing screen not much bigger than an index card. The resulting projection (see photograph) is decipherable, but not sharp. The display, based on a matrix of 100 by 100 points, can produce only five shades of gray plus black and white.

Key to the LCD's operation is the fact that liquid crystal molecules are in different conditions in each of their three states—and, what is more, the positions taken on by the molecules in the nematic phase remain "frozen" into place in the smectic. In both states, the crystal molecules are parallel. The differ-

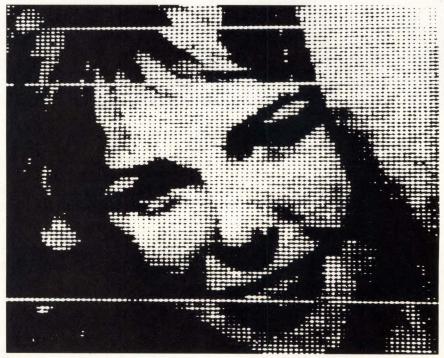
ence is that in the smectic phase, the centers of gravity of the molecules line up in parallel, equidistant planes; in the nematic phase, though, the centers of gravity are randomly distributed. In the isotropic state, however, the crystal molecules themselves are randomly distributed.

Sensitivities. Nematic liquid crystals are sensitive to electrical fields, whereas such fields have no effect on crystal in the smectic phase. On the other hand, smectic crystals are sensitive to temperature.

The resistances heat the crystal to the point where it passes from the smectic through the nematic into the isotropic phase. As the heat is cut off and the temperature drops, the crystals move back through the nematic into the smectic state. As they change, the molecules do not line up again and the result is a crystal that diffuses light.

Lined up. However, if an electrical field is applied to the vertically arranged electrodes during the cooling process, the molecules do line themselves up and the result, in the smectic state, is a single transparent crystal. Although the ambient temperature is significant, Thomson says its experimental screen operates at between 15° and 30°C.

To display an image on the screen,



TV or not TV. Experimental LCD from Thomson-CSF produces a projected TV picture by exploiting the properties of the smectic, nematic, and isotropic states of liquid crystals.

Adac System 1000 handles a ton of I/O functions.

In its simplest form, the System 1000 functions as a low cost peripheral expander to minicomputers. When incorporating a DEC LSI-11 microcomputer, it acts as a stand-alone data acquisition and control system or as a remote intelligent terminal.

No other data acquisition system comes close to offering so many analog and digital input and output modules. Functional analog cards communicate directly with thermocouples, load cells, strain gauges, isolation amplifiers, transmitters and strip chart recorders to name a few. Discrete cards communicate with switch contacts, relays, thumb wheel switches, pumps, motors and many other devices.

A single System 1000 provides up to 700 high level analog input channels, or 128 analog low level input channels, or 700 digital I/O functions. For even greater capacity, a bus repeater card allows additional System 1000s to accommodate as many modules as



Electronics international

signals corresponding to each point along a row are fed in parallel to the columns as the rows cool in sequence. The drive signals range between 15 and 20 volts, way below the kilovolts needed for a CRT.

The process happens so fast, the researchers claim, that rows can be changed in less than 60 microseconds (compared with 64 μ s for a TV line). There is no flickering at low speeds because liquid crystal in the smectic state has, in effect, a built-in memory; that is, the molecular positions do not change until the row is heated again.

In the experimental screen exhibited at the Paris show, an analog-to-digital converter is used to feed a video image onto the screen. As the LCD is developed, says Michel Hareng, director of the visualization lab within the Thomson research labs, a fully analog device will replace the converter and do away with the concomitant logic problems.

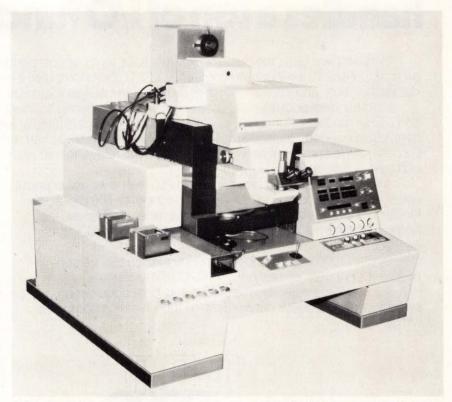
First, though, Hareng says, Thomson will concentrate on increasing the number of rows and columns to achieve a much more sharply defined image. He says work is already under way on a larger matrix, although he refuses to say just how much larger. Eventually, with the larger matrix and the all-analog device, he envisions a smectic LCD that will be virtually an integrated circuit. -Kenneth Dreyfack

Japan

Deep UV unit projects fine lines

Japan's VLSI Cooperative Laboratory has developed a deep-ultraviolet-light unity-magnification reflex projection unit that can print line widths as small as 1 micrometer with alignment accurate to within 0.3 μ m. The lab did the basic design and set the system's specifications, with the detailed design and fabrication carried out by Canon Inc.

Key to the new aligner is a 2-kilowatt deep UV point source. This xenon-mercury lamp is very stable



Going deep. Unity-projection machine developed by Japan's VLSI Cooperative Laboratory and Canon magnifies deep UV light into an arc-shaped beam to print lines as narrow as 1 μ m.

and efficient. Three concave mirrors preceding the photo mask magnify the light into an arc-shaped beam having a uniformity of better than 97%. This shape is used because it minimizes the aberrations of the projection mirror system between the mask and the wafer.

In general, the optical projection system is similar to that used by Perkin-Elmer Corp. [Electronics, July 21, 1977, p. 81], but it is different in detail.

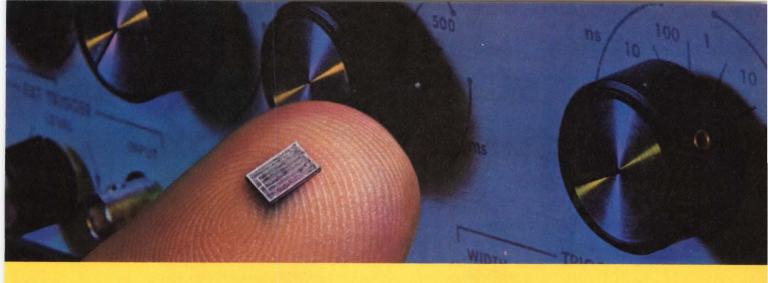
Exposure of an entire wafer of up to 5 inches in diameter is performed in a single process. The mask and wafer are aligned on a frame. The frame, mounted on air bearings for smooth operation, then moves past the 1.5-millimeter-wide beam at a constant speed. This causes the beam to sweep across the mask and wafer, thereby exposing the wafer.

Alignment. Before exposure, a filter shutter is placed between the light source and the photo mask. The filter stops deep ultraviolet rays, preventing exposure of the resist on the wafer, but passes visible light and thus permits alignment of the

mask and wafer through the system's microscope. After alignment, the filter shutter is removed.

The mask is fabricated on a fused-quartz substrate, which is transparent to deep UV light. In contrast, the glass usually used for masks is completely opaque at the 200-to-260-nanometer wavelengths employed for exposure. Fused quartz is more expensive, but since the masks never touch the wafers, they should last indefinitely. The resist used is polymethyl methacrylate (PMMA), and the metal is chrome.

An automatic parts feeder and an automatic laser alignment system permit processing of 60 5-in. wafers an hour. Although designed for operation at deep UV wavelengths for lines widths of 1 µm, the aligner can also be operated at ordinary UV wavelengths of about 360 nm for printing 2-µm line widths. Masato Nebashi, executive director of the VLSI Technology Research Association, which is the parent of the cooperative lab, says he expects Canon to start taking orders for commercial systems this fall. -Charles Cohen



Gain huge savings - in dollars and inches by replacing bulky conventional oscillators with tiny IC circuits.

While conventional oscillators (function generators, waveform GENERATORS, VCO'S, ETC.) COST UP TO SEVERAL HUNDRED DOLLARS, A SINGLE-CHIP IC OSCILLATOR CAN LITERALLY DO THE SAME JOB...AND FOR AS LITTLE AS \$1.72. All you give up for this tremendous reduction in cost and size is a certain degree of regulation in the output, and a variety of knobs and controls. But let's be realistic —for most applications, the IC oscillator is perfectly adequate. Its small size and low price makes the alternate approach quite impractical.

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Despite its small size, an IC chip really does contain every operating section of a traditional function generator. Consider a typical semiconductor oscillator, the XR-2206. On-chip you find the oscillator circuit (to generate the basic periodic waveform); the wave shaper to give you a clean sinewave; the modulator section (for AM capability); and an output drive amplifier. Basically the selfsame circuitry you'd re-ceive if you bought a standard oscillator or benchtop function generator hundreds, even thousands of times as big as the IC.

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oscillator will generate a combination of eight different types of output waveforms: triangle, ramp, sawtooth, squarewave,

sinewave, pulse and FSK (frequency-shift keying) outputs, each with its own appropriate range of applications.

Just the item for sweep generators and sweep modulators.

The sweep generator, with its output hodge-

podge of frequencies, can be a complex device. Yet it's a circuit easily built with ICs. A triangle-, ramp- or sawtooth-wave generator (XR-2207) modulates another oscillator (XR-2206) set up for voltage-tofrequency conversions. And presto! You have a functioning pocket-size sweeper.

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Where space is at a premium, the solidstate precision voltage-controlled oscillator (XR-2209) comes to the rescue with banners flying. It more than meets the functional accuracies required, saves pounds and inches, and shaves dollars too.

Audio test equipment too.

Low cost is the prime requisite here, and once again the IC oscillator comes through for the design engineer. Solidstate sinewave generators (XR-2206 or XR-8038) are ideal, low-cost, simple solutions that often can offer a size and power advantage perfect for the test or hobby

Digital communications, including data-interface or acoustical-coupled MODEMs.

The FSK oscillator is tailor made to solve this design dilemma. Modern designers, particularly those dealing with computer and data-processing systems, are continually put upon to squeeze more capability into ever decreasing amounts of space. Where board space is tight, the IC FSK oscillator (XR-2206 or XR-2207) is magnificently effective in compressing a complex function into a nutshell. You wind

up with inches of real estate for really important things such as more

memory.

Digital testers, logic circuits, on/off gating. Naturally, there's an IC oscillator for the purpose. This time one with a pulse output (XR-

2206 or XR-2207). All the same advantages you find in other applications—size, cost, low power requirements—apply here as well. In short, regardless of where you need to use an oscillator or function generator, there's an outstanding chance you can find a solid-state device to do the job and make you a hero in the bargain.

Beware. Only one company produces a complete line of IC oscillators.

With a stable of five different circuits, Exar boasts by far the industry's broadest choice of IC oscillators. From low cost, easy-to-use devices to high performance function generators, the line is summarized in Table 1. Check them out, find the one best suited for your use, then make the shrewd move to solid state. Exar's Function Generator Data

Book contains technical articles and application notes. To request your copy, write on your company letterhead to your nearest Exar representative or to Exar, 750 Palomar Avenue, Sunnyvale, California 94086.

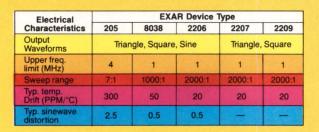


Table 1. Exar's line of IC Oscillators.



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In the graphics system shown, the input device is the HP digitizer (9874A), the mass storage is the internal dual tape drives, and the output is the HP 4-color plotter (9872A). You can interface System 45 with virtually any instrument found in the scientific



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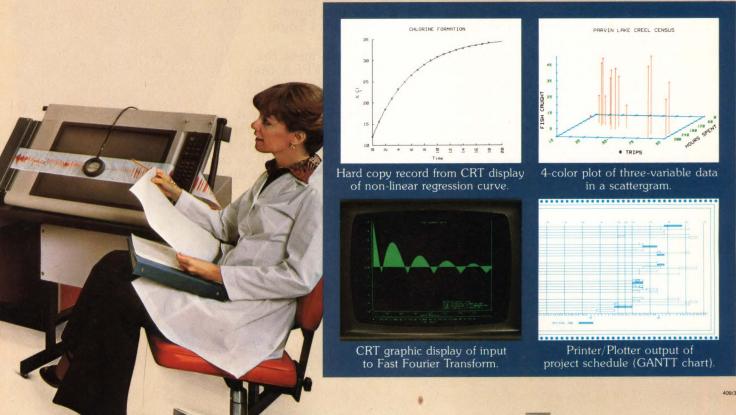
or engineering environment. All interface cards, cables and I/O slots are designed for quick "plug in and run" operation.

In addition, the System 45 Enhanced BASIC language allows you to upgrade any peripheral—internal printer to line printer, CRT graphics to 4-color plotter, tape drive to floppy disk—by simply changing one statement with no other software modification.

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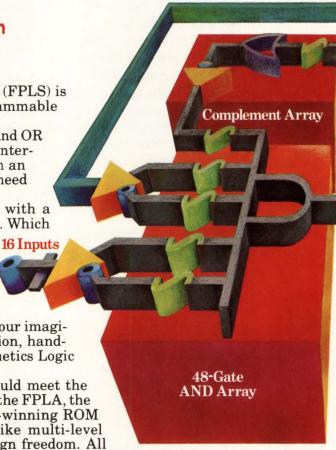
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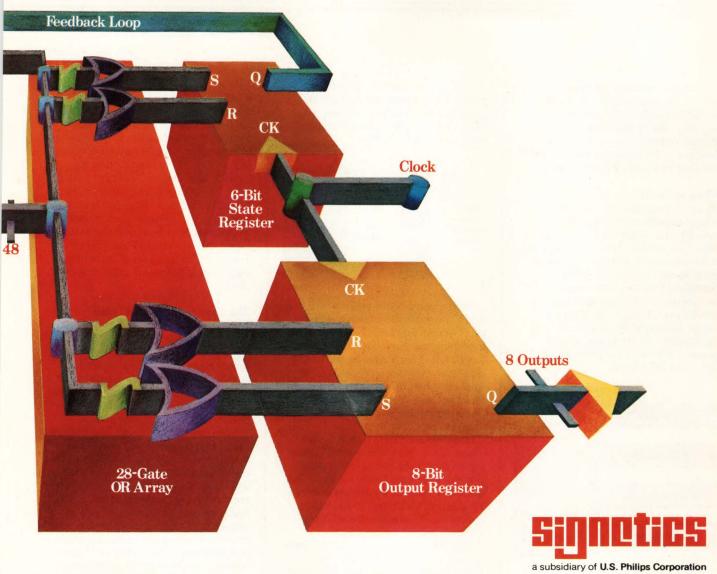
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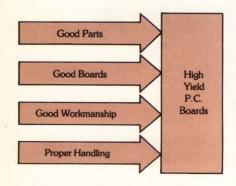
^{*}Two models available for each device: Open collector or three-state.

THINGS TO CONSIDER BEFORE YOU MAKE A DECISION

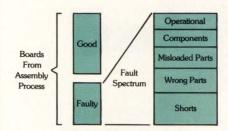
Is automatic testing a panacea? With today's PC volume and complexity, it's not so much a panacea as it is a necessity. But to implement a test solution requires a thorough understanding of the available test systems and your production environment.

When to test?

That's as important as how. The cost of fault identification increases dramatically with each production step. Thus, you want to catch faults as early in the production process as possible, but it doesn't necessarily follow that extensive incoming parts inspection is the answer. Your real goal is high turn-on rates in final test. That demands high-yield PC boards. And as the diagram below shows, several factors including good parts go into high-yield PC boards.



A PC board assembly process will produce anywhere from 20% to 80% good boards. A typical number is 60%. Of the faulty boards, a fault spectrum might look like this:



With a good board yield of 60% and no PC board testing, even a simple product with five boards would overload final test. Nine out of ten units would fail. This makes board level a good place for thorough testing. For this is the first opportunity to locate faults across the entire fault spectrum. But which tester is for you?

Choosing a circuit board tester.

There are no simple answers to selecting an automatic circuit test system. But, from our experience, we know that these are some of the factors involved: Production yield, test yield, fault spectrum, PC volume, board type, and anticipated new products.

Will the system test for the spectrum of faults that you will encounter? Will it generate component level diagnostic information? Will it test present and future board types and do it fast? Is it easy to expand and adapt to changing requirements?

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Over two million boards worth of experience.

HP's new Automatic Circuit Test Systems are the result of our extensive in-house experience with automatic circuit testing.

In fact, we were spending such large sums on dedicated equipment and manual test stations that back in 1970 we developed an automatic circuit test system called Optest I. This system, along with its more recent companion Optest II, is still in operation today. Optest I and Optest II are now testing over 100,000 printed circuit boards annually. Our new circuit test system is, in reality, a third-generation product, which originated from over eight years' experience in actual in-use operation. Today, HP is using 46 of these new automatic test systems within our own plants.

The case for in-circuit plus functional testing.

The marketplace has many potential test solutions. You can choose from simple shorts testers to completely automated systems. From testers that measure components in-circuit to functional test systems that verify dynamic performance of complete circuits.

HP's new 3060A Board Test System (\$74,000* for standard operational system) is an advanced system that combines the latest in-circuit technology with functional testing. It includes a comprehensive software package for fast program development. It is a proven package, which combines ease of use with flexibility to handle tough test problems. The addition of functional testing to in-circuit testing may provide a relatively small increase in board yield. But that small increase can



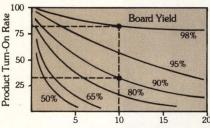




ON AUTOMATIC TEST EQUIPMENT.

result in large improvements in product yield, as shown below. For example, in a ten PC board product, increasing board yield by only 8% (from 90% to 98%) will leverage product turnon rate from about 35% to 80%. That's a large payoff, and an excellent reason to consider HP's 3060A.

PRODUCT YIELD VS. PRODUCT COMPLEXITY



Product Complexity (# of Boards)

The standard 3060A has a full set of analog and digital functional testing tools for testing most analog, digital or combined boards including at-speed testing of microprocessor-based boards using signature analysis techniques.

Some boards, such as large complex logic boards, will benefit from the use of HP's DTS-70 Digital PC Board Test System (\$90,350* for standard operational system). This simulator-based tester tells you how effective your test programs are and identifies the portion of the circuit not completely tested. This is important feed-back permitting better program development. A useful tool in R&D, the DTS-70 can model your designs and help you produce better products. Your test engineer will appreciate its ability to

model feed-back loops, find open traces and identify intermittent faults.

Just as important, the DTS-70's power and flexibility comes from its controller, the HP 1000 Computer System. Using a Real-Time Executive operating system, you can simultaneously test PC boards and develop new programs. As your testing needs expand, two more test stations and several programming terminals can be added without the expense of additional computer power. The operating system is compatible with data-base management software to keep track of your test data and help you better manage your production. The DTS-70 will easily fit into your long range computer network plans providing distributed processing and communication to your data processing center.

The bottom line.

Can automated PC board test equipment save you money? Again, there are no simple answers. But it has saved us money and chances are it will save you money, too, if any of these conditions exist in your plant: high PC volume, complex boards, production testing backlog, low turn-on rates of complete systems, high in-process inventory costs and high warranty costs.

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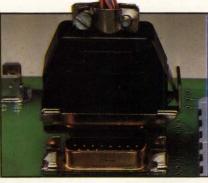
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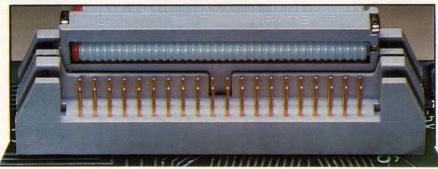
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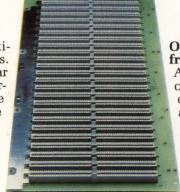
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Tunnel diodes flying high

Reliability and simplicity of supposedly forgotten technology make it ideal for satellite communications

by Harvey J. Hindin, Communications & Microwave Editor

Although the research money and hoopla for microwave amplifiers center around gallium-arsenide field-effect transistors, most of the wave amplifiers in communications satellites use germanium tunnel diodes, which were supposedly obsolete years ago. It appears that even the new birds—in the 14-gigahertz band—will be served by tunnel diodes.

It's all due to their simplicity, low power drain, and linearity. These, combined with a reliability so great that none of the 102 diodes used in Intelsat satellites has failed in 2 million device-hours of operation, makes for an almost irresistible combination. Contrary to popular opinion, the tunnel-diode amplifier is adequate both for the present 6-GHz family of satellites (noise figure of 5 decibels) and for the forthcoming 14-GHz generation (6-dB noise figure), even though the noise figure of FETs is 1 dB or so better.

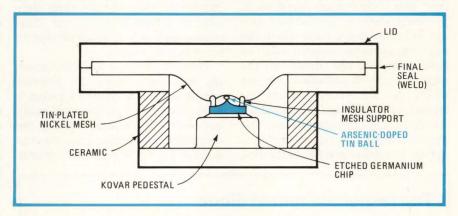
This success is due to an understanding of the tunnel diode's unique failure mode and the establishment of a screening technique that differs markedly from the conventional burn-in process. The work was done by Akos G. Revesz, senior staff scientist, and Paul L. Fleming, device physics department manager, at Comsat Laboratories in Clarksburg, Md.

Under stress. "Germanium tunnel diodes are subject to an internal mechanical stress that depends on subtle variations in the fabrication process, which may significantly vary from one device to another," says Fleming. "This stress may start a plastic deformation—known as creep—in the germanium, which

results in eventual deterioration of the diode characteristics."

Creep is intimately related to the way the diode is made, the Comsat researchers found (See "The neglected tunnel diode"). In a typical tunnel diode, the arsenic in the

arsenic-doped tin ball forms the n-doped region on the surface of the p-doped germanium chip. The tin ball is attached to a wire mesh and separated from the chip by two insulating supports. The chip must be etched so that the diameter of the



Construction. The typical germanium tunnel diode has a mechanically delicate germanium chip, tin ball, and nickel mesh junction. Internal stresses in this region cause partial or total amplifier failure, but a screening process culls out the susceptible diodes.



Probing the news

resulting pinnacle is only about 2.5 micrometers for a 6-GHz device and even less for higher-frequency diodes.

It turns out that there are large variations in the shape of the pinnacle and the position of the tin ball. The soldering of the mesh electrode to the tin ball also varies. Analysis of the mechanical stresses showed that even minor deviations from the mechanically ideal symmetrical mesh cause substantial mechanical stresses, since the junction area is very small. Comsat concluded that the diodes have an inherent built-in stress with a magnitude that varies in some unknown way.

Going bad. The diodes go bad by showing an increase in valley current. This is the current that flows in the diode when the applied bias voltage increases to the point where the negative resistance region is about to end, returning the diode to the normal forward diffusion current mode. As the valley current increases, the diode negative resistance decreases. In extreme cases, the negative resistance region may disappear altogether and the diode dies,

says Comsat's Fleming.

It was found experimentally that the valley current of a faulty tunnel diode increases with applied heat. "Apparently," says Fleming, "mechanical defects are generated" by the heat.

These defects are caused by plastic deformation of material that is time-dependent as well as thermally activated. In fact, there is an incubation time above which the defect density greatly increases.

Acorns. A theoretical study of this phenomenon led the Comsat researchers to conclude that a relatively small change in mechanical stress on the junction results in a change of up to five orders of magnitude in the creep incubation time. In the typically small junction of a microwave tunnel diode at the 25°C operating temperature of a satellite, the creep incubation time shrinks from decades to a fraction of a year. This occurs with only a small change in force on the junction.

Problems increase with the operating frequency. Since the junction area is smaller, a force that causes a given stress at 6 GHz produces much more stress at 14 GHz, reducing the creep incubation time. Therefore the demand for mechanical perfection of

the tunnel diode understandably increases greatly.

Explaining how much depends on a given tunnel diode's internal mechanical structure, Fleming says, "Since the internal diode construction at the junction can vary greatly, the internal stresses can also be very different. Their different sensitivities to creep reflect the variation in builtin stress."

Although annealing may allow substandard diodes to recover by relieving internal mechanical stresses, it is inconvenient. What was needed was a test or prescreening procedure to cull out bad or potentially bad diodes before they were used.

Timing. Simple burn-in of the diodes was insufficient to ensure adequate satellite lifetime because the valley current change was not detected. So Revesz proposed a more elaborate procedure using the temperature sensitivity of the incubation time to isolate high-stress diodes by measuring changes in the valley current.

This is done by subjecting the diodes to a carefully calculated temperature for a period that is equivalent to a specific mechanical stress over the seven-year projected satellite lifetime. Any diode with a change in valley current greater than 10% is rejected.

The results could not have been better. In one test, says Fleming, no failures were experienced in a screened group, whereas 10% failed in an unscreened group.

Not only have tunnel diodes been used in 15 Intelsat birds, but they are in at least 20 others, including Comstar, Anik, and Westar. They are scheduled to appear in Intelsat 5, at 14 GHz, where, according to Richard C. Mott of the Comsat Laboratories microwave laboratory, they will provide oscillation-free gain and noise figures of about 14.30±0.10 dB and 5.60±0.05 dB, respectively, performing across the 14.00-to-14.50-GHz band.

This state-of-the-art performance, Mott says, was achieved with the help of computer-aided design and is typical of what the diodes can do. The devices come from Aertech Industries Inc., Sunnyvale, Calif., at present the only supplier.

The neglected tunnel diode

Tunnel diodes—Leo Esaki's brainchild of the 1950s—never lived up to expectations because semiconductor device technology quickly bypassed them. Germanium-based and made by an alloying technique, they could not compete with silicon planar technology, which is suitable for inexpensive mass processing of devices. Silicon planar became the process of choice after the development of successful surface passivation of silicon by silicondioxide films. These films could also be used as a mask during the dopant diffusion process. Though tunnel planar diodes have been made, electrical noise problems have limited their use.

Since the production volume has been small, research and development have been at a minimum and the device technology—except for reliability considerations—has not changed much since the early days. Yet the simplicity of the tunnel diode has made it useful. Requiring only a direct current bias for operation as a negative-resistance amplifier, it consists of a narrow junction between heavily doped p and n regions. Electrons can easily penetrate the potential barrier across this junction by the so-called tunneling process.

When the forward bias on the diode is increased, the current increases, and then decreases, with voltage. With still further increases in the forward voltage, the normal diffusion current—as in the case of a standard p-n diode—takes over and the current increases again.

The region of interest, where the current decreases with increasing voltage, provides the negative resistance useful for amplifiction. Since the tunnel diode is a single radio-frequency terminal device, a circulator is required to separate the incoming signal from the amplified output signal.

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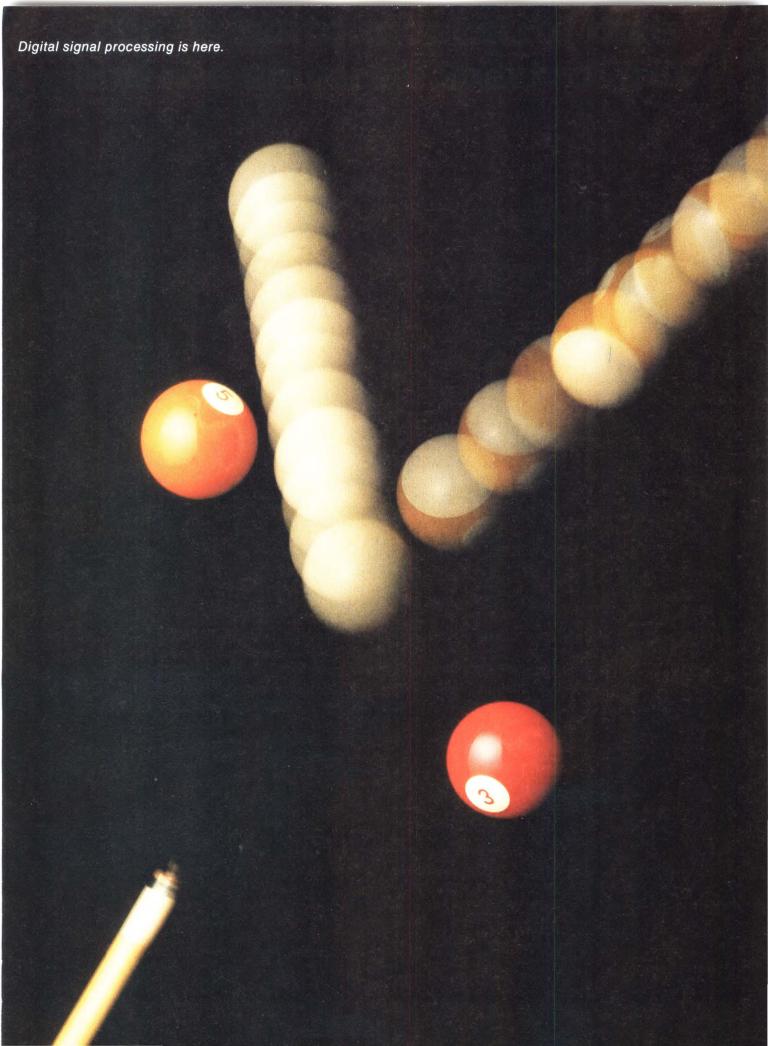
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Microsystems

STD bus leaves gate fast

Smaller, less costly solution from Mostek and Pro-Log has found a ready market as well as quick peripheral support

by John G. Posa, Microsystems & Software Editor

What amounted to a calculated risk about eight months ago by Mostek Corp. and Pro-Log Corp. has turned into a good-sized market with other companies moving in quickly to help exploit it.

The risk involved a decision to design and build a new bus for microcomputers despite the fact that the Multibus, the S-100, the LSI-11, and a slew of support products for them already existed. But Mostek of Carrollton, Texas, and Pro-Log of Monterey, Calif., moved ahead with their joint design on the theory that big modules clogged with large-scale integrated devices often spelled overkill. Thus was born the STD bus [Electronics, Aug. 31, 1978, p. 41].

STD boards are small, almost tiny, measuring only 4.5 by 6.5 inches, and they interface via an inexpensive 56-line edge connector cleanly segmented for 8-bit data, a 16-bit address, power, and control. What's more, because the idea and the first boards came from two sources simultaneously, the developers reasoned that potential supporters would be less afraid to get started.

It turns out that they were right. There is a market, especially in industrial and process control. Sixteen bits are still 8 too many for some applications, and the users like the small size and price of the modules as well as the ability to pick and choose only the functions they need. Although Mostek and Pro-Log remain the primary sources for central-processing-unit and memory modules, several companies have elected to bring out peripheral support, and others are following.

Analog Devices Inc. in Norwood, Mass., and Data Translation Inc. in

Natick, Mass., are helping to interface the STD bus with the real world. Data Translation just announced four data-acquisition cards [Electronics, April 12, p. 255], and Analog Devices is putting the finishing touches on a board that has 16 analog inputs and 2 analog outputs. It was challenged to stuff all it wanted into the confines of an STD module, so a new analog-to-digital converter was designed, and the board will use only monolithic integrated circuits. "Future boards will be more processor-independent and intelligent for remote operation," predicts Barry Glasgow, marketing manager for microcomputer peripherals at Analog Devices.

Specialists. Smaller companies, lacking ready access to leading-edge analog and digital processing, are putting together more specialized interfaces. Industrial Dynamics Inc., Parma Heights, Ohio, has built a stepper-motor controller that gives an STD CPU software control over the pulse rate and start and stop ramping. Don Davenport, the firm's president, says future products will include a temperature controller for heating and curing, a dc motor controller, and a 4-kilobyte electrically erasable programmable readonly memory (EE-PROM) module.

Another company with plans for an EE-PROM board is Microcomputer Applications Inc. of Woburn, Mass. It already has a dual asynchronous receiver-transmitter module and a clock-timer that "emulates the Intel 8253-5 programmable interval timer chip," according to Ernest Frohring, the firm's president. "We will concentrate on specialized ac-line interfaces in the future," he says. The

first, due next quarter, will connect to solid-state relays from Motorola Inc.'s Semiconductor Group and Opto 22, Huntington Beach, Calif.

Ziatech Corp. of San Luis Obispo, Calif., has also decided on a marketing strategy. "I'd like to put together a poor man's HP2240A," says Bert Forbes, president of the company (Hewlett-Packard's 2240A is a 128-channel measurement and control processor). So Ziatech's first STD module interfaces the bus with the IEEE-488 instrument bus (HP calls it the HP-IB and the 2240A connects to it). The next board will have eight dry-reed relays.

"Most of our boards will look like memory, with jumpers for mapping," says Ron Daubenspeck, an applications engineer at Micro-Link Inc., Carmel, Ind. Orders are now being taken for a four-channel asynchronous-synchronous receivertransmitter with on-board interrupt control.

A keyboard and display controller will be its next STD board. It will really be two boards in one: the controller will mate with the STD bus, and the 16-digit alphanumeric display and 64-key keyboard will be on a separate card to facilitate connection to a front panel. Still more future support will include an a-d converter using the 7109 chip from Intersil and a printer driver to control a dot-matrix mechanism.

In one interesting application, Kris Brown and Jerry Jeffress in San Raphael, Calif., are using STD boards to control the animation for the sequel to the motion picture "Star Wars." Jeffress, who received an Academy Award for his work on the film "Close Encounters of the

	MAKERS O	F STD-C	OMPAT	IBLE E	BOARDS	S					
Board type	Functions	A	and Devices	Inc.	Mes. Namics	Mic. Flectronic Syst.	Mic.	Mo	Pro.1	Ziate	45.
Single-board computer	CPU with RAM, ROM, and I/O	1		-	1	1	1	-			/
- Jo board dompater	Dynamic RAM	-		-	-		1		,		
	Static RAM		-				-		•		
Memory	RAM/ROM		-	-			-				
	ROM only	1	1 2				-		•		
	Nonvolatile (EE-PROM)										
Memory and I/O	E-PROM/UART	-						•			
	Serial I/O	-				•	•	•			
	TTL input				1 10 10				•		
Digital input/output	TTL output		10.10			4			•		
Digital input/output	TTL I/O		-		1		100	•	•		
	IEEE-488 interface		-				1000			•	
a same at 1	Transmission-line		1 2 /	-		0.0	4/10				
	A-d converter		•								
Union Standard of S	D-a converter										
Analog I/O	A-d and d-a		1		-						
A Trail The bould	Analog expander					1	11 11				
Control Land September	Ac-line monitor		2			100					
	CRT display				•	1	41.11	•		1.35	
	Floppy disk						TIME	•	11 11		
	Cassette										
	Printer			1,000		•					
0	Direct memory access							•		1	
Controllers	Keyboard and display						1 90			13 17	
	Stepper motor			•			50 0	-10-0	14.6	14.11	
	Modem						25		Day P.	The field	
	Ac line	1						-	•	•	
	Temperature			•			1	Hum	11/14/1		
	Single step			7		1		•	24		
Hardwara anhanasmast	Floating-point math		11 2			T	11111		Frank		
Hardware enhancement	Real-time clock and timer	1		1 8/11	P.A.		•			11/1	
	Calendar clock	-	-	-	+						

Third Kind," is handling the hardware and Brown is doing the software. "We're using STD modules from outside suppliers and we are building some of our own," says Brown. "We were probably one of the first to get Data Translation's converters."

To interface with a Hewlett-Packard cartridge tape deck, they designed their own IEEE-488 interface using Intel's 8291 and 8292 chips. They put Advanced Micro Devices' Am9511 high-speed math processor to work on another card for "the scaling of the axes," and they built

their own stepper-motor driver to position the cameras. "We have to control the cameras and keep track of the movements," says Brown.

Growing. Both Pro-Log and Mostek are stepping up production and rounding out their families. "We have one to two cards a month under development," comments Ken Marks, marketing technical support manager at Pro-Log. "About the only support product not yet provided is a bubble-memory module," says Ron Baldridge, a Mostek marketing manager.

If the STD concept has a limita-

tion, it would have to be that the bus itself could never be upgraded to accept 16-bit data or a direct addressing range larger than 64 kilobytes. All 56 of the signal lines are currently dedicated, so expansion means rethinking definitions.

So far, Z80 CPUs have been put on the STD bus by both Pro-Log and Mostek. Pro-Log also offers cards employing the 8085 CPU and, just recently, the 6800. But there is no reason hybrid chips—16-bit processors with 8-bit buses like the 6809 and the 8088—cannot be put on the STD bus later.

Probing the news

Medical electronics

Rf used to fight cancer

Experimental fever therapy in which body is heated to as much as 50°C shows encouraging results

by James B. Brinton, Boston bureau manager

Medicine is attacking cancer with electromagnetic radiation, from a few megahertz to microwave frequencies, and the results are encouraging. The heating produced by radio-frequency radiation often weakens and sometimes kills cancer cells. In addition, it also seems to enhance other cancer therapies.

Such heating is part of a larger thrust in cancer treatment called hyperthermia, or fever therapy. It is based on the simple technique of heating either a tumor or a whole body to a temperature that normal cells can withstand but cancer cells cannot. The use of hot baths and other "direct" heat treatments is not new, and interest in rf heating has been growing steadily in recent years because it offers good temperature control and because its effect can be as localized as the physician desires.

Pluses. There are other advantages, too. According to Dr. Howard M. Shapiro, chief of cytokinetics at Boston's Sidney Farber Cancer Institute, hyperthermia "doesn't 'depress' the bone marrow [impairing the body's response to disease], and it won't lead to nausea, vomiting, or hair loss, as will ionizing-radiation therapy. Nor is there any interference with surgical wound healing."

What's more, he continues, "it is suitable for use with high-risk or feeble patients. Its side effects are few and modest, and those that exist are different from those of other cancer therapies [making it possible

to combine other therapies with hyperthermia]. Finally, rf heating sometimes can be used on inoperable tumors. It's interesting stuff."

It becomes even more interesting in the light of research results like those of Dr. J. Y. Kim and his associates at New York's Memorial Sloan Kettering Cancer Center. Kim combined rf heating at 27.12 MHz with ionizing-radiation therapy in the treatment of malignant melanoma, a tumor type known for its resistance to ionizing radiation. He

treated two groups: one with the combined therapies, and another with ionizing radiation alone, with the latter group acting as an experimental control.

Kim heated the tumorous tissue to a minimum of 42.2°C, holding the temperature for 30 minutes just prior to radiation therapy. Six months after this combined therapy, 16 of 18 tumors in nine patients had "completely responded," but only 1 of 8 tumors treated with radiation alone had responded.

A tailored system

"We hope the BSD-1000 will give researchers the kind of experimental control they need to generate convincing results," says Ted V. Jensen, director of marketing for the manufacturer, BSD Corp. Introduced in late February by the Salt Lake City, Utah, firm, the BSD-1000 may be the first system especially developed for radio-frequency hyperthermia research. It combines a microprocessor-controlled rf system with cathode-ray-tube displays and hard-copy printout of experimental parameters.

Its rf system covers a range from 10 to 2,500 megahertz, making it possible for the researcher to control the depth of rf penetration, and thus the depth of heating. Lower frequencies penetrate more deeply; higher ones are restricted to areas near the surface of the body.

Temperature is measured in the tumor with nonmetallic thermistors. Their output is fed to a Z80 microprocessor, which in turn controls rf output. The result is temperature control to within ± 0.1 °C.

To avoid confusion with ambient fields or rf reflections, the BSD-1000 comes with a walk-in screened room lined with rf-absorbing material. Large enough for studies on large animals or humans, its rf-tight construction also allows experimentation at all frequencies without interfering with other uses of bands not reserved for medical use.

BSD is selling the system for about \$117,000. That's not much above cost, but the company is philanthropically supported, making profit less of a concern. "We want to keep price down," says Jensen, "and make hyperthermia available to as many researchers as possible." He expects to sell or lease about 20 systems this year, with early units going to the Loma Linda (Calif.) University School of Medicine and the University of Utah.

What about clinicians? "Of course, some of these systems are going to make their way into clinical use; we can't stop that. But we are selling a research tool, not a treatment," he says, making a distinction that may be more important to the regulators of such devices at the Food and Drug Administration than to cancer victims.

A report by Harvey J. Hindin in the April 12 issue (p. 85) explored research on microwave detection of tumors. This article discusses experimental treatment of tumors.

Kim's results could mean two things for future cancer patients. First, some radiation-resistant tumors could be treated more successfully using the combined approach. Second, with hyperthermia, smaller doses of radiation might be required than are needed now.

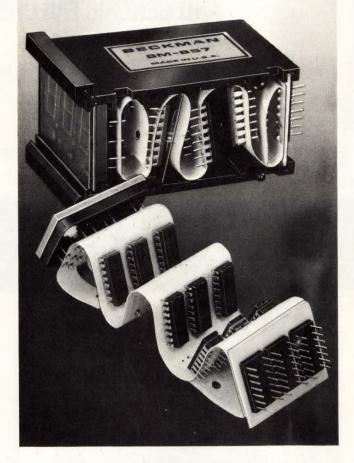
The research of Drs. J. A. Dickson and S. A. Shah is typical of animal studies done using rf hyperthermia. Working in England at the cancer research unit of the Royal Victoria Infirmary, Newcastle-upon-Tyne, the experimenters implanted tumors in rabbits and let them grow until some had become as large as 22 millimeters. Others spread throughout the animals' bodies. Using a 13.56-megahertz rf heater from Critical Systems Inc., Palo Alto, Calif., they heated the tumors to 50°C for 30 minutes. In the following six to eight weeks, 10 of 15 tumors regressed, and metastasis, or cancer-spread sites, disappeared as

Dickson and Shah prefer rf hyperthermia over other forms, most of which they find slow, cumbersome, and ineffectual. The pair also tried electrocoagulation hyperthermia and found it rapid, but temperature was hard to control and the coagulator left a slow-healing, easily infected wound. There was only one regression in 18 rabbits treated with electrocoagulation.

Explanations. There are several theories that try to explain the effect of hyperthermia. Shapiro offers another. Many tumors have concentric layers of tissue. "The center is often dead, he notes, "and is usually surrounded by a layer of so-called dormant cells with little circulation. Around this is a fast-growing surface layer. If you raise tissue temperature, the heat will be carried away from normal tissue far more efficiently than it will be removed from the tumor. Where you have heat, you have changes in cell ph and other factors which can kill cancer cells. That's the important thing."

If the news is all good, why isn't medicine rushing to use hyperthermia? There are several reasons, but most critical is the chicken-and-egg problem with available equipment: there is so little rf hyperthermia equipment available that researchers

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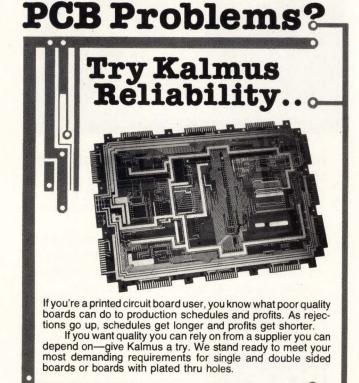


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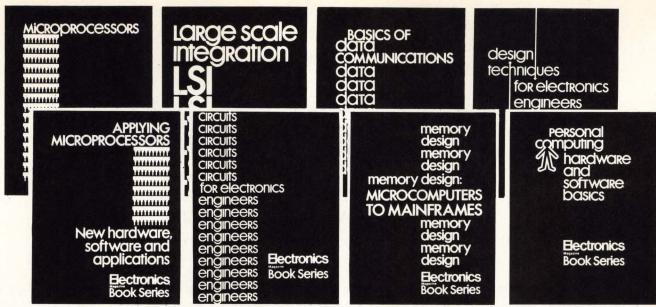
have used jury-rigged microwave ovens, ancient diathermy machines, and costly custom systems. And although the experimental results have been exciting to many, the variety of equipment used makes it hard to generalize from published reports and thus difficult to design effective hyperthermic treatment. This holds back clinical use of hyperthermia, and the lack of a market holds back equipment producers. (See "A tailored system").

There are also questions of technique. For example, should the tumor alone or the whole body be heated? Some research indicates that whole-body hyperthermia may be less effective, and thus one group favors localized heating. Another group figures that there is always a risk of cancer having spread by the time it is discovered and that whole-body hyperthermia is better, as it would treat unknown cancer sites.

Finally, some fear that rf heating may help spread a cancer even as it kills it. Because circulation in the normal tissue surrounding a tumor increases with temperature, doctors are afraid that cells might slough off a tumor and be carried in the blood to another part of the body. This is an obvious area for future research.

In use. Meanwhile, a few physicians are trying to use rf hyperthermia. For now, it is a treatment of last resort, used largely on terminal patients when other therapies have failed, or on individuals with otherwise untreatable cancers—say, large tumors involving the head that cannot be removed surgically.

That seems to be about all that can be done until there is either more experimental data available or more rf-hyperthermic equipment on the market. "What's needed are firm research results based on wellcontrolled experiments," says Shapiro. "Hyperthermia looks good, but it still has a lot of people to convince. Blue Cross/Blue Shield won't pay for rf hyperthermia treatments and the Food and Drug Administration will have to pass on the effectiveness of any hyperthermia equipment sold for clinical use." Until then patients may just have to wait.



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Computers

New architecture goes with flow

Data-flow concept developed at MIT uses parallelism to do away with RAM, program counter, CPU

by James B. Brinton, Boston bureau manager

After 12 years of study, researchers at the Massachusetts Institute of Technology are getting ready to build a different kind of computer. The data-flow computer exists only on paper, but by late summer, an engineering prototype might be operating and pointing the way to future machines that could be smaller, cheaper, and 50 to 100 times faster than traditional designs.

Almost all currently available computers use a random-access memory, a program counter, and a central processing unit (CPU). Instructions and data are fetched from

the memory in a sequence monitored by the program counter; successive operations like add, compare, and multiply are performed in the CPU until the program has run its course. But most problems have a lot of parallelism; their solution involves many operations that could be done simultaneously. And that's where the data-flow concept comes in.

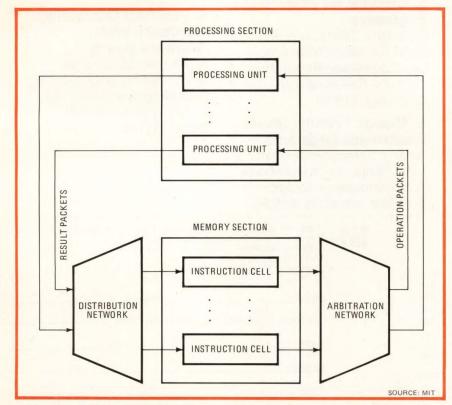
Old and new. A data-flow machine has no central processor. Instead, it has a processing section with tens, hundreds, or thousands of processing units—each perhaps equivalent to a simple arithmetic and logic unit or

an input/output processor. There is no RAM, either. Instead, there is a memory section with a potentially large number of cells, each holding operating code, operand, and destination address. The usual synchronous clock, program counter, and storage registers are absent, too. Instead, a packet-switching system called an arbitration network directs the output of a memory-section cell to an appropriate processor unit of the system.

Each processor unit crunches its part of the problem and sends a "result packet" consisting of a cell address and an operand to a distribution network, which routes it to a cell for storage.

The leader of the group that has developed MIT's data-flow concept is Jack B. Dennis, a 47-year-old professor of computer science and engineering and head of the computation structures group of the Cambridge, Mass., institute's Laboratory for Computer Science. Dennis once sketched a data-flow machine 100 times more powerful than a \$10 million IBM 360/91. The paper machine would have been about as compact as a large mini-"I could have installed it in my office," says Dennis—and would have a 200megahertz instruction rate, although Dennis points out that the figure is a little misleading. Not only are many instructions being executed almost simultaneously, but also data-flow instructions do more than instructions used in typical computers.

The hardware. Dennis's group is finishing the hardware design for a data-flow machine, and so far it seems as if data flow and large-scale integration were made for each



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Probing the news

other. "In our early machines, we might use only one or two types of processing unit, perhaps a maximum of four if we need the specialization," he says.

He goes on to project as many as 512 processing sections, each with several processing units, for a possible total of 2,048. There would be a similar number of cell blocks, composed of 16-byte-deep cells and logic. To switch and steer the operation and result packets, there would be networks of two-by-two-port routers, each consisting of a pair of multiplexers, 8 to 16 bytes of buffer memory, and control logic. A dataflow computer could contain thousands of routers in its arbitration and distribution networks. These relatively simple circuits are good candidates for LSI.

When the hardware is assembled, the group will use its VAL language to program the machine. VAL, for value-oriented algorithmic language, "is complete enough now to allow coding of large scientific programs," Dennis says, adding that he expects VAL to develop into a general language with wide applications.

Industry response. Meanwhile, industry is keeping a low profile, according to Dennis. "Only Texas Instruments has an in-house dataflow program, to my knowledge," he says, noting that TI also has an inhouse application for a fast computer in its seismic data-processing business. And Burroughs Corp. is supporting a form of data-flow work at the University of Utah.

If data flow is not only potentially cheap because of its LSI implementation, but lightning fast as well, why isn't there more industry interest? It is not because data flow is unsuited to general-purpose work. Dennis points out that "IBM and others have a large investment in existing software, and for data flow to be most useful, programs now written in Fortran, PL-1, and Cobol would have to be rewritten in something like VAL." The alternative would be to develop a translation system to convert standard programs into something that would take advantage of data flow's parallelism.

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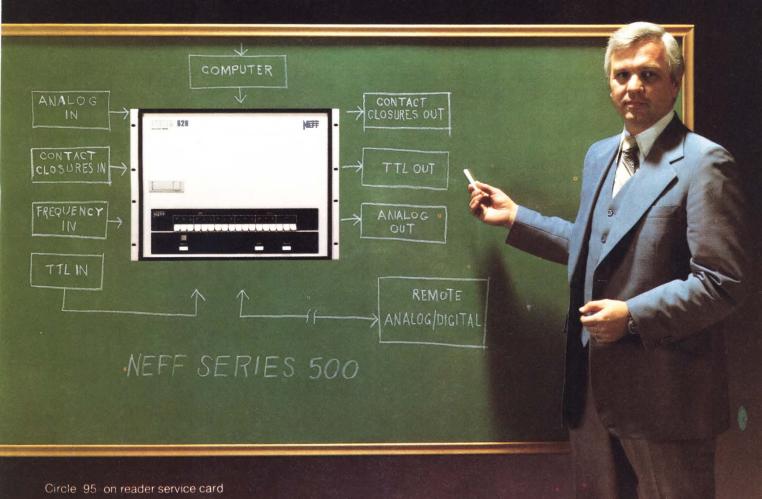
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Optoelectronics

Display meeting looks at computers

Half of papers to be presented at SID conclave are related to that area; show also is heavy with papers from overseas

by Howard Wolff, Assistant Managing Editor

Trend watchers will have a field day in Chicago early next month at the annual meeting of the Society for Information Display. For the meeting—officially it is the International Seminar/Symposium and Exhibition, to take place May 7–11 at the Chicago Marriott—will put the spotlight on two important tendencies in display technology in particular and in technology in general.

In the first, the movement is toward computers. "About 50% of this year's papers are tied up with computers in one way or another," says program chairman Philip M. Heyman of RCA Corp.'s David M. Sarnoff Laboratories in Princeton, N. J.

The second trend, a more ominous one, has to do with the direction of research and development in the United States. "Several years ago," says Heyman, "about 20% of the papers were from foreign countries. Last year it was 35%, and this year the figure has jumped to 50%. Where is American R&D going?"

Syllabus. All told, the conference will be packed with nine technical sessions, two panel discussions, and four tutorial seminars. Though the subjects of most of the nine sessions are predictable—flat panels, cathode-ray tubes, projection systems, and the like—one will deal with nonimpact printing and another with high-density information storage.

In the session on nonimpact printing, three out of five papers are from Japan, two by a team from Oki Electric Industry Co. Those engineers,

Slim picture. Flat-panel vacuum fluorescent display from Ise Electronics Corp. of Japan will be described at SID annual meeting.

led by S. Nakaya, will discuss their use of low-cost paper with flat-bed scanning for a gray-scale recording system for picture facsimile or TV hard copy; they will then describe a system of high-speed thermal recording in which parallel drivers heat the head elements instead of multiplexing them.

In the session on high-density storage, Hsu Chang of the IBM Research Center in Yorktown Heights, N. Y., will review the potential of bubble and charge-coupled devices; K. K. Bulthuis of Philips Research Laboratories in Eindhoven, the Netherlands, will describe an optical disk system based on a gallium-arsenide diode laser; R. A. Bartolini and A. E. Bell of RCA's Sarnoff labs will review playback media for available optical-disk recording systems; and a method of photographic replication of full-bandwidth NTSC video signals that have been laser-recorded on thin metal films will be described by D. G. Howe, H. T. Thomas, and J. J. Wrobel of Eastman Kodak Co., Rochester, N. Y.

LCDs. The busiest technical session is the one on liquid-crystal displays, with eight papers. Two Britons, I. A. Shanks and P. A.

Holland of the Royal Signals and Radar Establishment in Malvern, Worcs., will describe an addressing method to drive LCDs in single-value displays [Electronics, March 29, p. 70], and two Americans, A. L. Berman and G. Kramer of Beckman Instruments Inc. in Fullerton, Calif., will outline a method for constructing light-field pleochroic LCDs.

Five papers are from Japan: from Nippon Electric Co.'s team, led by T. Ueno, will come a description of a cholesteric dye display with dark characters on an electrically driven background; and a group from Hitachi Ltd. led by K. Odawara will discuss an 80-character alphanumeric system for computer terminals. A twisted nematic layer device will be described by T. Uchida, Y. Ishii, and M. Wada of Tohoku University in Sendai, and two-frequency addressing of a 56-line twisted nematic display using an improved material will be the subject of a group from Suwa Seikosha Co. of Nagano-ken led by M. Hosokawa. Finally, C. Tani heads a Nippon Electric team that, working with O. Kogure of Nippon Telegraph and Telephone Public Corp., produced low-power storage matrix LCDs.



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4N27	10	1500	n n	1
4N28	10	500	"	1

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4N32	500	2500	Photo Darlington	1
4N32A	500	2500	11	1
4N33	500	1500	н	1
IL-100	1000	2500	High Speed 75 nS	1
IL-101	1000	1500	High Speed 200 nS	1
ILCT6	20	1500	Photo Transistor	2
ILD74	12.5	1500	п	2
ILQ74	12.5	1500	II .	4



THE LIGHTS FANTASTIC



The Great Micro Power Op Amp Race: It's easier to win when no one else begins.



© PMI 1978

Lewis Carroll loved competition. In *Alice in Wonderland* the action frequently unfolds as some form of game or race.

The most nonsensical of all is the Caucus Race. As Alice discovered, it's a race where everyone wins, which is the same thing as saying that no one wins. In the I.C. business, there's a lot of that going around.

As the Dodo explained to Alice, for a Caucus Race you simply mark off a racecourse in a circle, and then everyone lines up around the course. The competitors begin running when they like and they stop when they like, so that it isn't easy to tell when the race is over.

In Carroll's Wonderland, the race lasted until the Dodo cried, "The race is over!", following which the

runners stood panting around the circle asking, "But who has won?"

"Everyone has won," said the Dodo, "and all must have prizes."

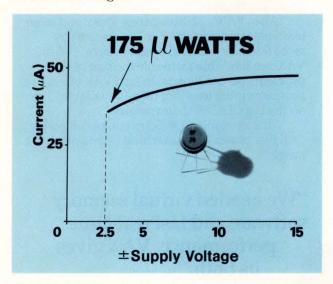
In Linear Wonderland, there has been kind of a Caucus Race going on for some time in the development of micropower operational amplifiers. A lot of people have jumped into the circle, run for a while and then stopped, so that the industry lost track of who was running or when the race would end.

But now it's official. PMI has declared, "The race is over!", as it announces the *OP-20*, the first *precision* op amp that runs on just microamperes and can be powered from either dual or single voltage supplies!

Of course, as Alice herself says, it's much easier to win a race when no one else begins. No one else *really* began in this race, either. A few thought they had and even thought they had won when they offered micropower op amps, without precision performance. That's about as absurd as calling the Mad Hatter's watch a watch, when it tells you the day of the month, but not what o'clock it is.

The Winner!

Look at these specifications and you'll see why we've declared the *OP-20* the winner in a race no one else has even begun.



Only 175 Microwatts are needed to supply the OP-20—that's 35 microamperes from a ± 2.5 volt supply. And the supply current stays below 50 microamperes when powered by dual supplies to ± 15 volts.

In Linear Wonderland, everyone thinks you've got to trade off a lot of performance in order to get down to micropower supply levels. But PMI knows you don't win races that way. That's why with the *OP-20*, offset voltage is typically 100 microvolts and input offset voltage temperature coefficient is extraordinarily low at 1 microvolt/°C. At 15 nanoamperes, input bias current is low, too.

Sound like a winner? We're not even done yet.

Open loop gain is over 1 millon; common mode and power supply rejection ratios both exceed 110 dB.

So who is the real winner in this race?

Everyone out there in Linear Wonderland who wants a precision micropower op amp with single supply voltage. And beware the Jubjub Bird and the frumious Bandersnatch who try to mislead you by saying their Op Amps achieve the same results by being programmable. In the language of Linear Wonderland, which is not far removed from Carroll's "Jabberwocky," that means that they couldn't give you what you want, but if you play around with it long enough maybe you can do it yourself. The next time they come whiffling through the tulgey wood, smite them with your vorpal sword!

Versatility is a key to the OP-20's success with designers. It can be powered with either a single 3 to

30-volt or a dual ± 1.5 to ± 15 -voltage source and the common mode input voltage swing is wide, from V- to within 1.5 volts of V+.

There are a trillion sockets in Linear Wonderland and the OP-20 will fit in many of them. It's at home in 4132, 741, and 4250 op amp sockets and it comes in TO-99 cans or minidips. It can also be bought as a 42 x 68 mil chip for hybrid applications.

Explore all the things you can do with the *OP-20*. After all, you can get them right now from your dis-

tributor's stock.

The OP-20 is PMI's newest winner in Linear Wonderland.

As the White Knight said to Alice after the Red Knight rode away from the battle, "it was a glorious victory, wasn't it?" He knew that victory is still sweet even when no one else puts up a fight.

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OP-20GJ	-25/+85°C	TO-99	150	4.00
OP-20HJ	0°/+70°C	TO-99	300	3.00
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OP-20HP	0°/+70°C	Mini-Dip	300	2.20



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and a full-blown operating system."

Dr. Herb Schwetman, Assoc. Professor Dept. of Computer Science Purdue University West Lafayette, Indiana

Purdue's Department of Computer Science is involved in researching operating system performance, programming languages, and computer system security.

Because their experimentation requires heavy interactive use, they needed an alternative system to augment time-sharing on a CDC 6500.

Dr. Herb Schwetman, Associate Professor, explains what made Digital's VAX-11/780 so attractive. "We were intrigued because VAX provided a lot of the features and performance of a central facility—but for a lot less money."

Since Purdue's research involves state-of-the-art technology, VAX's advanced architecture and software were especially appealing. "The operating system is set up very cleanly," says Dr. Schwetman, "Processes can operate independently. And that's a very good way to do it."

Also, VAX's 32-bit address space and large main memory give the Purdue researchers more flexibility. Dr. Schwetman says, "With VAX, we'll be able to double the size of the problems we can look at. In fact, VAX offers user programs more memory than is available on the big CDC 6500 downstairs."

"It's amazing," Dr. Schwetman concludes, "All this power—in a machine in this price range."

"We needed virtual memory software and fast real-time performance. VAX gives us both."

> Gary Willis, Program Specialist Advanced Technologies Engineering Laboratory Ground Systems Department General Electric Company Daytona Beach, Florida

> > At the Advanced Technologies Engineering
> > Laboratory of its Ground
> > System Department,
> > General Electric designs
> > color visual systems for
> > flight simulators, primarily
> > for the military.



The application demanded operating system software that could handle static simulation; but real-time performance was important, too. After a number of tests and benchmarks, General Electric decided on VAX.

Gary Willis, Program Specialist, tells us, "If you can imagine emulating a roomful of simulation hardware, you can see why we needed a virtual memory operating system. But since we have to compute a new image every 30th of a second in our real-time application, we also needed a lot of number crunching. VAX gives us both."

The VAX/VMS operating system and realtime dynamic performance are only part of what impressed General Electric. Says Willis: "Most military contracts require FORTRAN, and we're very pleased with what VAX gives us - very fast, very efficient FORTRAN, with super execution times."

According to Willis, VAX software is also

getting high marks on ease-of-use.

"Our people are very pleased with how easy it is to translate FORTRAN programs from the PDP-11 series to VAX. Also, our programmers like the HELP command – especially those who are just getting used to Digital equipment."



"We were very impressed with the maturity of the VAX operating system. Everything that's supposed to work, works."

Harry Hill, Program Manager Ford Aerospace & Communications Corp. Western Development Laboratories (WDL) Div. Palo Alto, California

Ford Aerospace performs large double precision floating point scientific computing for a variety of government projects.

When it was time to move to a larger computer, WDL's Harry Hill, Program Manager,

admits they were apprehensive about committing to a product as new as Digital's VAX-11/780.

"We were originally very leery of the new machine," says Hill, "Because it traditionally takes years to develop maturity. But the price was so good that we went ahead, and it's been very successful."

One feature that made VAX particularly attractive for Hill's application was the powerful virtual memory. He tells us: "By going to VAX, we were able to eliminate memory mapping and let the machine just sit there and crunch numbers. It saves time and cuts down on the chances of messing something up."

Hill is also impressed with VAX's interactive and batch capabilities. "The multi-stream, multi-queue batch is one of the best systems we've ever seen."

The programmers' reaction? Says Hill, "Everybody is amazed."

Digital's VAX-11/780 represents the first truly integrated approach to hardware and software architecture. The result is one of the most advanced systems on the market. Extremely powerful, yet extremely easy to use.

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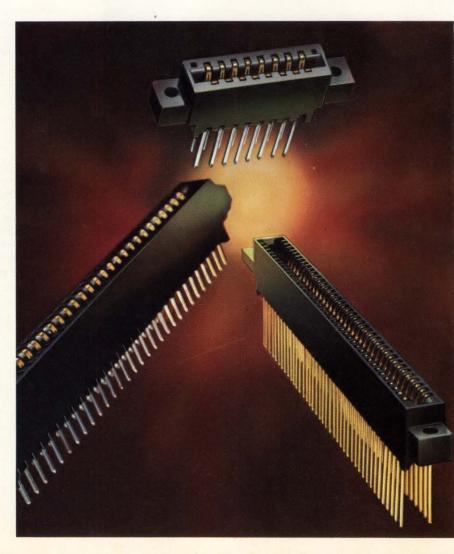


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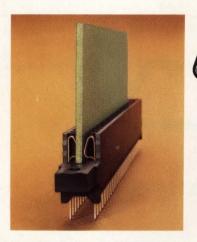
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Insulation Resistance: 5,000 Megohms (min. after humidity test)

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4-530396-7	43 Pos.	3 Hi Wrap Type Post
4-530396-8	50 Pos.	3 Hi Wrap Type Post
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1-530841-8	30 Pos.	0.187 Solder Tail
1-530841-9	36 Pos.	0.187 Solder Tail
2-530841-0	40 Pos.	0.187 Solder Tail
2-530841-1	43 Pos	0 187 Solder Tail

2-530841-1 43 Fos. 2-530851-2 50 Pos. **0.125" Centerline** 4-530825-6 28 Pos. 0.187 Solder Tail 3 Hi Wrap Type Post 30 Pos. 36 Pos. 4-530825-7 5-530825-0 4-530825-0 40 Pos. 50 Pos. 28 Pos. 5-530825-2 3 Hi Wrap Type Post 0.187 Solder Tail 0.187 Solder Tail 1-530842-7 1-530842-8 30 Pos 36 Pos. 40 Pos. -530842-9 0.187 Solder Tail 2-530842-0 0.187 Solder Tail 2-530842-2 0.187 Solder Tail 50 Pos.



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VN64GA Specifications



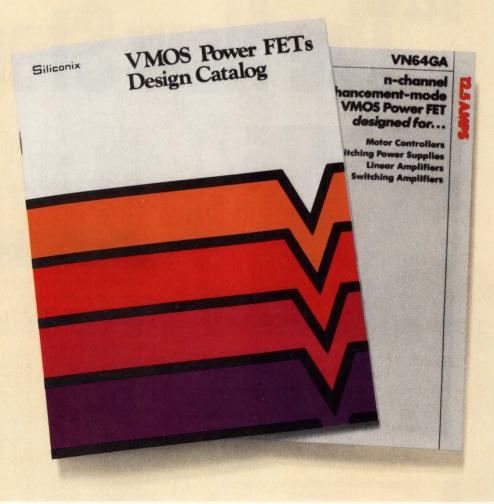
 $\begin{array}{ccc} \text{BV}_{\text{DSS}} & \text{60 volts} \\ \text{I}_{\text{D (on)}} & \text{12.5 amps} \\ \text{R}_{\text{DS (on)}} & \text{0.4 ohms} \\ \text{P}_{\text{D}} & \text{80 watts} \\ t_{\text{(on)}}, t_{\text{(off)}} & \text{45 ns.} \end{array}$

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Our new 12.5 amp VMOS power FET is here

Megabit bubble-memory chip gets support from LSI family

Dedicated control and addressing chips, sensors, and driver waveform generators ease system interface problems

by Don Bryson, Dick Clover, and Dave Lee, Intel Magnetics Inc., Santa Clara, Calif.

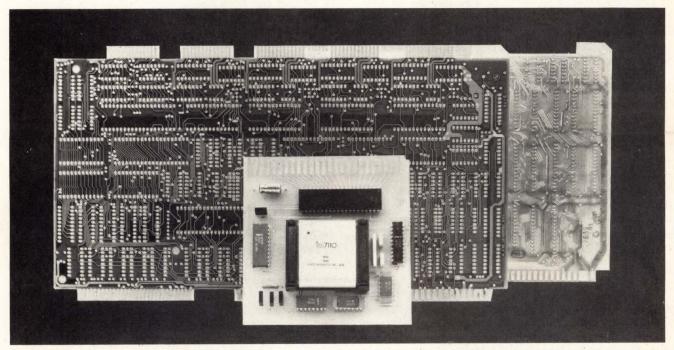
☐ Because of their potentially high density and nonvolatility, magnetic-bubble memory devices are destined to find diverse applications in areas ranging from low-performance terminals to high-performance mass-storage systems. However, to utilize the attractive capabilities of bubbles, the system designer must deal with an interface problem more challenging than that posed by semiconductor memories.

The designer, for example, must not only provide addressing and control logic for the memory device, but also precise current-pulse generation, low-level analog voltage sensing, and relatively high-current waveforms in a set of drive coils. For bubble memories to gain wide acceptance in the marketplace, therefore, their manufacturers must provide more than a memory device. An entire family of parts is needed to ease the designer's complex interface problem.

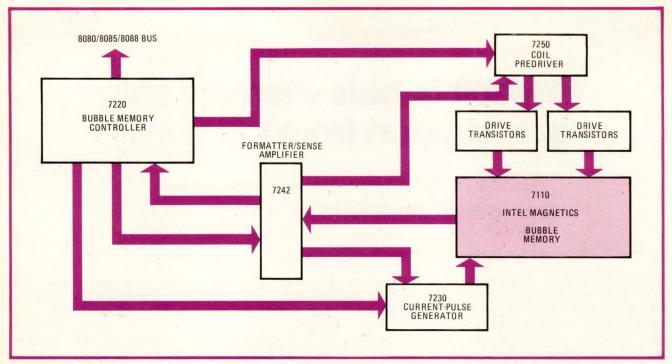
Now Intel Magnetics, a wholly owned subsidiary of

Intel Corp., has fulfilled these requirements with the introduction of a 1-megabit magnetic-bubble memory chip accompanied by a supporting family of large-scale integrated (LSI) circuits that not only provides an easy-to-use interface, but also retains the flexibility the user needs to configure a system according to his own requirements. Figure 1 is a block diagram of the generalized system concept developed by Intel Magnetics. Key ingredients are compatibility with the 8080/8085/8088 bus system, use of advanced LSI technologies, partitioning of control and data paths, and a degree of user programmability. Transparent handling of redundancy, automatic error correction, and power failure reset are built-in features.

Heading the family is the Intel Magnetics 7110, a nonvolatile, solid-state memory with a normal data capacity of 1,048,576 bits. The device includes additional memory that is normally devoted partly to error



Space saver. Availability of Intel Magnetics bubble memory and supporting LSI family of control and driver circuits reduce space, component count for 1-megabit bubble system by order of magnitude, replacing two printed-circuit boards, four 256-K modules, and about 85 ICs.



1. Minimum system. A complete bubble memory system with a storage capacity of 128 kilobytes can be implemented with only one 7110 bubble memory package plus four LSI devices along with two quad transistor packs. The entire system can fit on a 16-square-inch board.

correction and partly to extra storage in the form of redundant loops, to increase the yield of good devices. The accompanying interface circuits are the 7220 bubble memory controller, 7242 formatter/sense amplifier, 7250 coil predriver, and 7230 current-pulse generator. With these, designers can now begin product development using the memory, without concern for drive and interface details. They can treat memory and support electronics as a unique new mass-storage element.

The memory is expected to be used initially in microprocessor applications requiring 128 kilobytes to 2 megabytes of storage. These include terminals, word-processing systems, telecommunications, and process-control wherever nonvolatile storage is required.

The basic components of Fig. 1 can be used to build a minimum system of 128 kilobytes in a 16-square-inch board space. For larger systems, up to eight magnetic-bubble memories (MBMs) can be interfaced with one controller for a megabyte of storage. Through the 7220 bubble memory controller the system interfaces directly with the Intel microprocessor bus systems, so the memory can be treated as a slave to 8080, 8085, 8086, or 8088 host systems. Key functions of the system include binary data organization, standard +12- and +5-volt power supply operation, flexible multiple MBM organizations, single-page (512 bits, or 64 bytes) or multiple-page data transfers, and built-in error correction.

A 1-megabit MBM

The 7110 is a serial-parallel-serial shift-register storage device with a binary page organization. Its storage elements are cylindrical bubble domains, 2.7 micrometers in diameter, occurring in a thin film of magnetic garnet material grown by liquid-phase epitaxy on a gadolinium-gallium-garnet wafer. After the film is

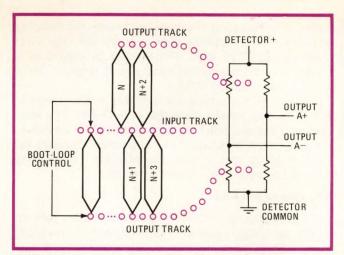
grown, wafer-processing is similar to that used with silicon. Standard photolithography creates conductive and magnetic nickel-iron patterns on the chip. The permalloy patterns form storage loops, input/output tracks, and control elements. The permalloy elements are the usual asymmetrical chevron patterns.

The resulting 2-square-centimeter chip stores 2,048 pages, each holding 512 bits in turn divided into two channels of 256 bits, or 64 bytes. Figure 2 shows one channel of the 7110's basic organization and illustrates the separate block-replicate, block-swap organization. There are 128 data-storage loops per channel divided into two sections of 64 data loops each. A page address is selected and the page is shifted to the starting location for a read or a write operation.

The first part of the read operation nondestructively replicates the bits of the page in parallel on an output track to feed a detector bridge. The bits are shifted serially through the bridge so that the maximum data rate is twice the shift rate. In the write operation, the bits for a new page are first written serially on an input track. Again the maximum data rate is twice the shift rate. The bits shift until they coincide with the bits of the page in storage to be replaced. A swap operation then exchanges the new page for the old at the address location selected.

The performance of the device is readily estimated from the shift rate. The initial product, the Intel Magnetics 7110, will have a shift rate of 50 kilohertz and a storage loop 4,096 bits long. Therefore, the average random access time of a page is about 40 milliseconds. The maximum data rate is twice the shift rate, or 100 kHz. Page read and write times for the 7110 each require a minimum of 327 shift cycles, or 6.5 ms.

From this, the average data rate is 78 kHz (512 bits



2. Organization. Basic bubble memory architecture has a serial-parallel-serial organization. Shown here in simplified form is one of two channels of the 1-megabit MBM. There are altogether 128 loops in each channel, plus a so-called boot loop whose function is to identify and keep track of the guaranteed-good loops.

per page divided by 6.5 ms). Most of the reduction from the maximum data rate is associated with the spare storage-loop overhead on the chip. Along with the 256 guaranteed data-storage loops holding the 512-bit pages, there are 64 additional loops. Sixteen of these are guaranteed good so an error-correction code of up to 32 bits can be appended to each 512-bit page. Up to 48 loops can be defective, so that in fabrication a few processing defects do not mean rejection of the chip. Defective loops can be isolated during testing so that they do not interfere with memory operation. Provisions are made in the support electronics to compensate for them. These spare loops, therefore, increase chip yield and hold down costs.

The boot loop

At the system level, the good storage loops and the spare loops must be identified so data is never entered into the spares. To handle this, the bubble memory chip has an additional loop, called the boot loop, that holds a loop-map code for that particular chip along with an index address code. When the system is turned on, the boot code is replicated at the detector. First the index address is located and sets up the address counter in the controller. Then the loop map is read and stored in the Intel 7242 formatter/sense amplifier (FSA). After this, page read or write can begin.

In operation, one page or a burst of pages can be read or written for a given system request. Upon completion, the bubble device itself can be stopped until the next request. This start/stop feature can reduce the average page access time in systems where successive page accesses are not random. Least recently used (LRU) and look-ahead algorithms can be used to put expected future pages at the locations corresponding to the start of the page read or write cycles.

Also at the system level the data rate can be increased by operating bubble devices in parallel. The Intel 7220 controller allows up to eight in parallel. With the 50-kHz 7110, the average bit rate then becomes 625 kHz. With two controllers and 16 7110s, the bit rate is 1.25 MHz.

	One magnetic- bubble memory cell (MBM)	Four MBMs	Eight MBMs operated in parallel	Eight MBMs multiplexed one at a time	
Capacity 128 kilobytes		512 kilobytes	1 megabyte	1 megabyte	
Average data rate	62.5 kHz to 125 kHz	250 kHz to 500 kHz	500 kHz to 1 MHz	62.5 kHz to 125 kHz	
Average access time	50 to 25 ms	50 to 25 ms	50 to 25 ms	50 to 25 m	
Power dissipation (100% duty factor)		20 W	40 W	11 W	
tandby power 1.3 W		3.7 W 7.0 W		7.0 W	
Board area	ard area 16 in.2		90 in.2	90 in.2	

Sometime in the future a 100-kHz MBM, the 7112, will be offered with twice the data rate. Table 1 shows the range of expected performance characteristics encompassed by the 7110 and 7112.

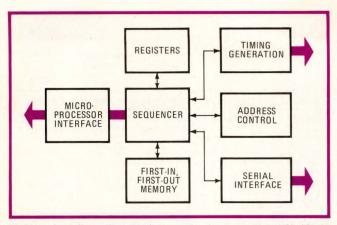
Support components

The user interface is provided by the Intel 7220 bubble memory controller (BMC). The controller is a 40-pin LSI device implemented in Intel's HMOS technology. Figure 3 is a block diagram of the 7220 BMC. Major functions of the controller are to provide the bus interface, to generate all memory system timing and control functions, to maintain memory address information, and to interpret and execute user requests for data transfers.

The heart of the bubble system is the 7242 formatter/sense amplifier diagrammed in Fig. 4. The FSA is a dual-channel device that can interface directly with both channels of the memory. Three key functions of the 7242 are sensing the low-level bubble signals, handling the redundant loops, and buffering data. In addition, the user may choose a circuit for detecting and correcting burst errors. The 7242 FSA communicates with the 7220 BMC via a serial bus, so that a 20-pin DIP may be utilized. The operation of the FSA is discussed in more detail later. An advanced n-MOS technology was chosen to incorporate sensing and data-handling functions.

A Schottky bipolar process was chosen to implement the Intel 7230 current pulse-generator (CPG) because of the relatively high peak currents required. The 7230 CPG interfaces directly with the 7220 BMC and the bubble memory device and provides the fast, high-current pulses required by the latter. It consists of a reference-current generator, a power-failure-sensing circuit, and 12 current sinks switched on or off by the 7220 controller. The chip contains a power-down circuit that shuts off the current sources whenever the chip is disabled. The 22-pin device's logic diagram is shown in Fig. 5.

Finally, the support electronics makes it possible to drive the coils of the bubble memory. The peak currents required in the coil are beyond the capacity of standard IC devices, so a coil predriver (CPD) that interfaces the 7220 controller and discrete transistors has been developed. The Intel 7250 CPD is a C-MOS device in a 16-pin DIP that translates the TTL outputs of the 7220 controller into high-voltage, high-current signals that can be used



3. User interface. The 7220 controller is a complex LSI 40-pin device that provides the interface to the system bus, generates all memory system timing and control functions, and supervises the execution of data transfer requests.

to drive transistors. The logic diagram of the 7250 is shown in Fig. 6. Quad transistor packs are used to drive each coil. V-channel MOS field-effect transistors are preferred for the drivers, since they are fast, require no bias currents, and have a built-in diode to commutate the coil current when the transistor is turned off. However, the 7250 CPD has the ability to provide up to 200 milliamperes of base current for bipolar drivers.

System features

Since the system designer is given a complete set of LSI parts, he can concentrate on higher-level system objectives, instead of having to learn the intimate details of bubble memory interfacing. He saves still more time by working with a standard bus already familiar to him, rather than designing counter circuits and trying to convert millivolt signals into TTL voltage levels. The system operates from +12 v and +5 v only, with circuitry to monitor these voltages. Should the voltages drop below acceptable levels, it will shut itself down in an orderly manner, so that integrity is preserved.

Even though the details of interfacing to the bubble device are hidden, the support electronics are flexible enough to accommodate widely different system designs. Figure 1 shows the minimum system—that is, it contains only one bubble device (128 kilobytes) and the required support electronics. Figure 7 is a block diagram of a larger system containing eight bubble memory cells. Each contains a bubble device, a 7230 CPG, a 7250 CPD, and two quad transistor packages. A single 7220 BMC can directly control from one to eight bubble memories.

Expansion to larger systems can be accomplished in two ways. In the first approach, provisions are made in the BMCs for paralleling controllers. This provides greater word width at the bus, and each controller can still accommodate from one to eight bubble memory devices. In the second, each support device has a chipselect pin so that banks of devices can be switched into or out of the circuit under external control. The maximum number of devices in each bank remains eight. In addition to these two expansion modes, the 7220 BMC also has a chip-select input so that entire subsystems may be multiplexed (or, more typically, located at different I/O

addresses). This form of expansion involves the decoding of I/O or memory-address lines to create the chip-select input for the 7220 BMC. The amount of expansion is limited only to the number, usually quite large, of I/O or memory addresses available.

Although eight devices are included in the system in Fig. 7, the user retains the option of accessing data from only one. The controller transfers data and commands to the FSA over a serial bus. The controller addresses the 7242 FSAs by means of a time-division multiplexing scheme that allows individual addressing.

The role of the FSA

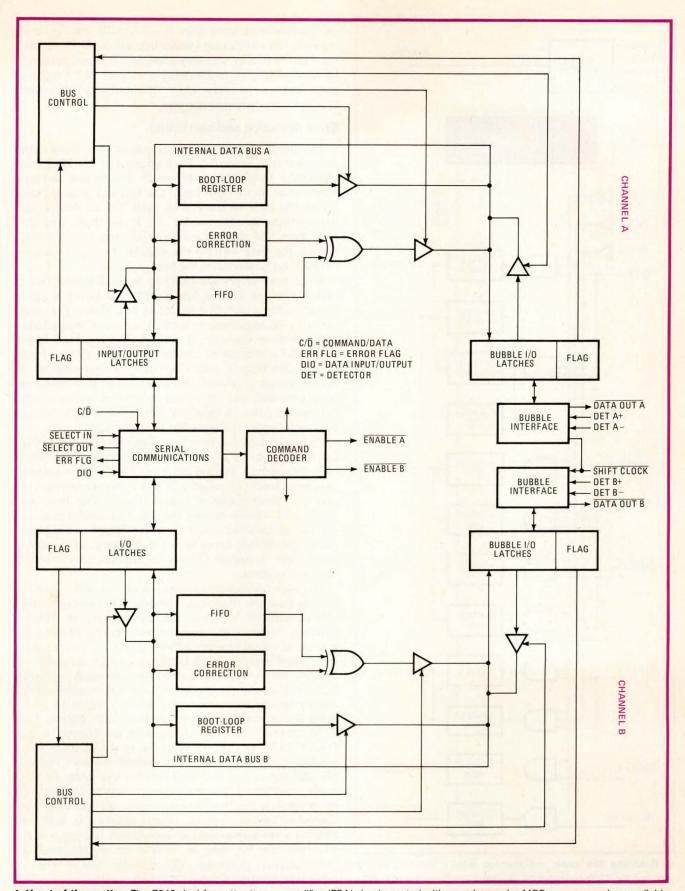
To communicate with the FSAs, the controller puts out a sync pulse that is passed in shift-register fashion along their daisy-chain configuration. Simultaneously, a data stream is put out on the serial bus. As each FSA receives its sync pulse, it examines the serial bus to determine whether it is being addressed. Note that each channel of the dual FSA can be individually addressed since the sync is passed internally from channel A to channel B. Commands are distinguished from data by a C/D pin controlled by 7220 BMC. The direction of data on the bus is determined by the mode the FSA has been set to by the controller. However, FSAs are forced to "listen" to the serial bus when a logic C/D line occurs.

Any FSA that is not addressed during a command automatically disables and removes itself from the bus. This action provides an added benefit, in that each FSA channel also has an enable output active only when selected. It is connected to the chip-select pins of the other support circuits, so each bubble memory device that is not needed for the present access remains powered down. The only restriction on the selection of devices to be accessed is that the number of channels to be accessed be binary (i.e., 1, 2, 4, 8, or 16) and that each multiple group be contiguous in the FSA daisy chain. For example, if the user's data rate requires that two bubble devices be accessed simultaneously, the two must be either devices 1 and 2 or 3 and 4, etc.

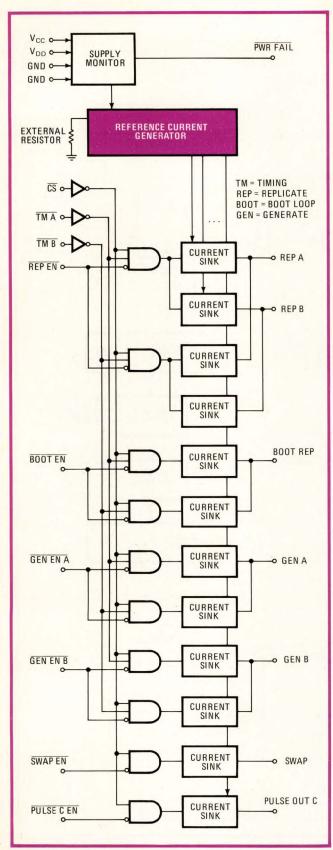
In any configuration, data is transferred in serial form and reassembled into an 8-bit byte by the 7220 controller. The serial bus operates at a minimum rate equal to 20 times the rotating field rate so that a bit of data can be transferred to or from each FSA channel during each field rotation. Thus a system containing a megabyte of bubble memory can be useful in low-data-rate, low-power systems as well as in high-performance systems. The partitioning of most of the data handling into the FSAs makes this flexibility possible.

It now becomes readily apparent why the FSA is considered the heart of the system: it enables the system to parallel as well as multiplex memory devices easily—something not possible previously with bubbles. All this is accomplished with minimum parts since the sense amplifier and redundancy handling are in the same package. Redundancy handling involves deleting bits read from defective loops on the bubble chip and inserting zeros into the data stream when writing to the bubble chip. This function is ideally performed by the FSA as the defective loops are different in each bubble device.

A map of defective loops is contained in the boot loop



4. Heart of the matter. The 7242 dual formatter/sense amplifier (FSA), implemented with an advanced n-MOS process, makes available many system functions that are required by the user, but handles them transparently. Besides permitting optional error correction and detection, the FSA makes it possible for the memory devices to be paralleled and multiplexed with minimum parts count.



5. Reaching the peak. Implemented with a Schottky bipolar process, the 7230 current-pulse generator produces the high peak currents required to power the 7110 MBM. It incorporates a power-failure-sensing circuit and a power-down circuit that shuts off the current sources when the chip is disabled.

on the bubble memory chip. It is normally read out and stored in the FSA during system initialization. Therefore, the 7220 controller sees only good data bits and need not be concerned with maintaining a map of bad loops for each bubble memory chip. Redundancy therefore becomes transparent to the user.

Error detection and correction

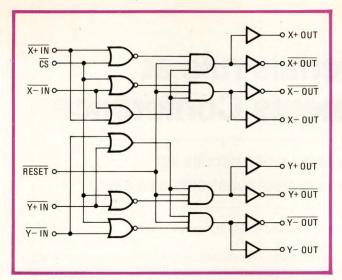
An additional function performed by the FSA is error detection and correction. Each channel of the 7242 FSA contains a 14-bit Fire code, which detects and corrects burst errors up to 5 bits long. The FSA can generate and attach the code to the end of each 256-bit data block when writing into the bubble cell. It can then check the code when the block is read and, if errors are present, correct the data—within the capabilites of the code—before it is transferred to the host.

Since most errors are likely to be in detection (soft) rather than in bubble loss (hard), repeating a read operation can generally be avoided. In addition, the error rate can be improved by several orders of magnitude, transparent to the user, if desired. The overhead loops required for storage of the code do not subtract from storage area (that is, each chip has a binary 1 megabit of usable storage). Should the user decide to forego the error detection and correction feature, or to implement his own, an extra 16 loops (32 bits) become available for data, error code, or page-address header and storage.

Not only does the user have flexibility in organizing his system, he can also choose his methods of transferring data across the system bus. The 7220 controller supports three: (1) polled I/O, (2) interrupt-driven I/O, and (3) direct memory access (DMA). The first two methods of transfer require that the host central processing unit be involved, i.e., data is transferred to a register in the CPU before being stored in memory. In the DMA mode, data is passed directly to host memory without host intervention.

High-performance systems with parallel bubble devices must use DMA since the data rate can exceed the I/O capabilities of most microprocessors. A bubble memory system with eight bubble devices running in parallel at a field rate of 80-kHz can achieve a maximum data-transfer rate of 160 kilobytes/s (6.25 µs/byte). A typical microprocessor instruction execution requires 2 µs. Since a transfer execution under CPU control would require several instructions, it is obvious that DMA operation is a necessity for higher-performance systems. The 7220 controller is designed to interface directly to an Intel 8257 DMA controller chip. For systems with moderate data rate where DMA is not desired, the DMA request pin can signal the host that data is available. In this mode (selected by the user by programming the controller properly), the DMA request pin is set whenever the controller first-in, first-out (FIFO) memory is half full (during a read operation) or half empty (during write). This pin can be used as a data, or second level of interrupt, that guarantees the host can read or write a minimum number of bytes (20) to the controller.

The last, and lowest, performance mode is provided by a status bit in the controller that indicates presence of data in the FIFO. The host could continually poll status



6. Predriver. The 7250 converts TTL outputs of the 7220 controller into the high-voltage, high-current waveforms used to energize the transistors that drive the coils of the MBM through quad transistor packs. The coil predriver can interface with either V-MOS FET drivers or can provide up to 200 mA of base current for bipolar types.

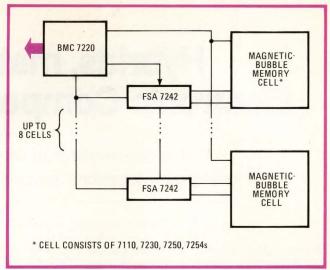
and output data when the FIFO is available, but this mode is useful only in the lowest performance system.

After power-up, the host must initialize the system. Communication with the controller is accomplished via a set of addressable registers contained within the controller. These registers are addressed by the host and written with information relating to the desired operating modes (for example, DMA is enabled, the number of data blocks is specified, etc.). The host must then issue a command to initialize. The controller proceeds to read the bootstrap loop of each bubble device (which is redundantly coded) and write the bad loop information into the bootstrap loop register contained in the corresponding FSA. The controller begins with the first FSA in the chain and continues down the chain in order until all devices have been initialized. Each bubble device is left in the home position (page 0 is ready to be read).

Sequence of events

After initialization, the controller, if enabled, interrupts the host and is ready for data transfers. The host writes an address into the controller registers, issuing a read or write command. The controller then takes over and accesses the desired page or pages of information. An interrupt is normally issued upon completion, but it may be inhibited by the user. An address is maintained and updated for each bubble device in the system, regardless of organization, within the controller. If a block transfer overflows the address boundary of a bubble device or devices, the controller will automatically switch to the next in the chain. A maximum of 2,048 pages of data can be transferred with a singlecommand sequence. Should a power-down occur during a transfer, the controller will automatically shut down the coil drivers in the proper sequence, if power remains at acceptable levels for about 100 microseconds.

The user requests data transfers by addressing a command/status register in the 7220 BMC. A large



7. Big system. This system diagram shows how the 7220 bubble-memory controller can be used to control up to eight bubble memory cells for a total capacity of 1 megabyte. Even more capacity can be attained by paralleling extra controllers. Additionally, the 7220's chip select input permits multiplexing entire subsystems.

number of commands are available to the user, including several that are useful for system diagnostics.

The most commonly used commands are:

- Initialize—performed after power-up in order to reset the system.
- Read—causes the selected pages of bubble memory to be accessed.
- Write—writes user data into selected pages of the bubble memory.

Read and write can be specified for 1 to 2,048 pages. In addition, a seek command lets the user predict his next read address, avoiding additional latency. However, in multiple-page read or write operations, consecutive page addresses are physically located so the next page is available immediately upon completion of the preceding operations. Additional commands include reading and writing of the bootstrap loop registers in the FSAs, or the bootstrap on the bubble chip, a software reset, and an abort command. Status bits provided to the user include a busy signal, an operation complete flag, a FIFO ready flag, and several error flags, including timing and correctable and uncorrectable error. Status of each FSA can be determined by the host processor with a special command. Interrupt masking lets the user decide whether he is interrupted by errors or by normal operationcomplete interrupts. The combination of error-correction capability, a versatile command set, and appropriate status flags also lets him perform on-line maintenance checks to enhance reliability.

The key design features incorporated in the Intel Magnetics MBM systems approach were chosen after a strong effort to define the appropriate markets for bubbles. Ideas from more than 200 potential customers were gathered and greatly influenced the choices of size, speed, and organization. Thus, two years after inception, the program will yield bubble memory products including development boards so customers can begin evaluating the 1-megabit bubble memory product line.

Hybrids, materials rule at **Electronic Components Conference**

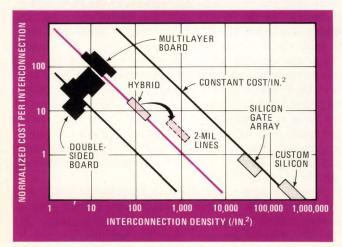
The requirements of very large-scale circuits set tone of many sessions; porcelain-on-steel substrates also star

by Jerry Lyman, Packaging & Production Editor, and Nicolas Mokhoff, Components Editor

☐ The "components" in "Electronics Components Conference" is a distinct misnomer this year. The annual conference, jointly sponsored by the Institute of Electrical and Electronics Engineers and by the Electronics Industries Association at the Cherry Hill Hyatt House, N. J., on May 14–16, is fast switching its emphasis from the discrete, passive components of years past to materials, manufacturing methods, and packaging, above all in relation to hybrid circuits.

In fact, thick- and thin-film hybrids are emerging as the best way to package very large-scale integrated (VLSI) circuits. For this reason, ECC has even seen fit to bestow an entire session on that supremely VLSI problem—what to do about the alpha particles that cause soft (transient) errors in the functioning of VLSI devices [Electronics, March 15, 1979, p. 85]. As it happens, the alpha particles that do the damage are generated within the very packages designed to protect the chips.

Still other ECC papers describe such ingenious new hybrid devices as a nonvolatile solid-state relay, a transformer equivalent, and high-voltage yet mass-producible silicon controlled rectifiers. The microwave potential of porcelainized-steel substrates is analyzed, and galliumarsenide MES FETs also come in for attention.



1. The cost of density. These graphs compare the cost and interconnection density of five packaging methods. The normalized cost per interconnection of multilayer boards and hybrids (5-mil lines and spaces) is the same. Hybrids, however, have 10 times the interconnection density of the multilayer boards.

As integration pushes chip densities to ever new highs, the packaging engineer must find the most cost-effective way of interconnecting these VLSI circuits. According to C. T. Goddard, head of the hybrid circuits department at Bell Telephone Laboratories, Allentown, Pa., thick- and thin-film hybrid circuits on ceramic substrates are the answer. He finds that 1 square inch of ceramic circuit costs about the same as, yet has 10 times the interconnection density of, 1 square inch of multilayer board containing two signal layers plus buried power and ground planes.

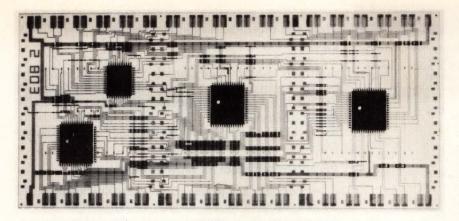
Hybrids rescue VLSI . . .

Figure 1 compares double-sided and multilayer printed-circuit boards, hybrids, and silicon chips in terms of their cost per interconnection. (This cost has been normalized by assigning 100 units of cost to the fourplane multilayer board already described.) Densest and least costly packaging occurs within the silicon chip, of course. But when the micrometer-wide lines of the chips must link up with the mil widths of the packaging world, the most effective solution is a hybrid with 5-mil lines and spaces of the type shown in Fig. 2, since its high interconnection density more than compensates for its intermediate cost. In fact, with 2-mil features, the perinterconnection cost of a hybrid falls to about 1/30 that of a multilayer board.

Goddard enlarges on his thesis by comparing the use of 68-pin chip-carriers with 200-pin hybrids in a design in which 25,000 gates must be interconnected on a 13-by-8-inch board. The chip-carriers hold 220 gates each, so that their board requires eight signal layers and the carriers barely fit in the allotted space. The hybrids can hold 2,000 gates apiece and fit easily on a board requiring only two signal layers—obviously a much simpler structure.

. . . despite soft errors

Though hybrid circuits may be the best way of packaging VLSI devices in terms of overall cost and density, they pose a problem in terms of reliability. Radioactive traces in their ceramic substrates generate most of the alpha particles that induce soft errors in the functioning of the dense chips. ECC therefore devotes an entire session to ways of measuring and compensating for the activity of alpha particles, a single one of which gener-



2. The superior hybrid. The four LSI chips on this two-layer substrate replaced 31 DIPs on a six-layer pc board, illustrating the cost-effectiveness of hybrid technology. There are about 500 gates on the 1.7-square-inch hybrid, and its interconnection density is about 100 gates/in.².

ates 1.4 million electron-hole pairs on a path 25 μ m long through silicon at right angles to the chip surface.

Of all the semiconductor technologies, n-channel metal-oxide-semiconductor is the farthest along the VLSI road. Its micrometer features and the minimal electrical difference between its binary 1s and 0s therefore make it the most vulnerable to alpha upset, points out Timothy C. May of Intel Corp., Santa Clara, Calif., in the session's first paper. The solution to this problem may lie in the chip, the package, or both, he says. Through the LSI level of complexity, the chip costs less than the package and a change in its design should be made to provide the solution. At the VLSI level, the package costs less than the chip and becomes worth improving also.

Table 1 summarizes the flux levels of the main packaging materials used in the semiconductor industry, including a rough estimate of the levels probable by the early 1980s. Having the largest area in parallel with the chip, alumina should be given priority for purification to the lowest possible flux level, though of course all materials next to the semiconductor chip must be guaranteed to a desired flux level.

However, there is a practical limit to the purification of any package material. As May says, it is the point beyond which the measurement of the flux level is impossible. Today's most sophisticated method—gamma spectroscopy—detects at best a flux of 0.001 to 0.01 alpha particle per square centimeter per hour, which is

only 10 to 100 times below the figure for the coldest (least radioactive) packaging ceramic now in use.

As for the effects of alpha bombardment on different VLSI circuit designs, May says the most vulnerable appear to be dynamic random-access n-MOS memories, some static RAMs, and in general any VLSI devices with low speed-power products and the ability to accumulate carriers. Possible remedies include: raising charge storage by decreasing front-end gate oxide thickness, reducing the duration of charge collection, and improving charge transfer, all with the goal of either dodging an alpha hit or minimizing its impact.

How to test

To evaluate the effectiveness of these different remedies, accelerated testing of the supposedly improved VLSI packages devices will be needed. (The alternative—large error-logging systems—is prohibitively expensive, according to May). Such testing would involve bombarding the packaged devices with intense alpha sources, producing $10^5 \ \alpha/\text{cm}^2$ -hr and up, in order to cause soft errors running around 0.1%/1,000 hr in a $0.1-\alpha/\text{cm}^2$ -hr package. Some other test method, though, would have to be found for packages whose device cavities are lined with alpha-barrier coatings.

In another paper, H. P. Gibbons and J. D. Pittman from Coors Porcelain Co. in Golden, Colo., agree with May's conclusions on packaging materials. They found

Material	Significance to device	Flux range (α/cm ² -hr)	1980s' range (α/cm²-hr)	Comments
Alumina	above die, in CerDIP low angle, in side-brazed ceramic	0.1-0.6	0.01-0.05	• screening of natural sources of alumina likely
Glass	low angle in CerDIP	1-60	0.01+	zirconia can be eliminated
	especially serious with full-glazed ceramic lids			may be "don't care" in some geometries, except for radon
Metal lids	• above die in side-brazed ceramic	≤ 0.01-0.5	< 0.01-0.05	sources of Kovar, Alloy 42 must be watched for uranium and thorium gold-plating controlled
Plastic packages	• above die	0.05-2.0	< 0.01-0.05	mainly due to silicon-dioxide filler; other fillers can be used
Coatings	• in contact with die	≤ 0.01	< 0.005	only useful if colder than package sources

Substrate type	Attenuation constant at 1 GHz (dB/in.)	Propagation velocity (% of free space)	50-ohr line width (in.)	
No. 1 porcelain on iron	0.9	48.0	0.010	
No. 2 porcelain on iron	0.75	44.0	0.010	
No. 3 porcelain on iron	0.68	45.5	0.012	
No. 1 porcelain on copper and iron	0.34	46.0	0.010	
No. 2 porcelain on copper and iron	0.32	45.0	0.010	
Alumina thin-film	0.28	35.0	0.00	

that ceramics, sealing glasses, and metalizing materials were all alpha emitters, but that ceramic has the worst effect on the chip, being in parallel with it and thus permitting line-of-sight alpha bombardment. Changing package geometry is not an effective cure. But coating the chip cavity walls with a material that blocks alpha particles and emits very few itself would virtually eliminate soft errors due to the particles. The package would be costlier but in some applications might be worth it in terms of improved reliability.

Further evidence

The lower limit of ceramic package alpha emission and how to reach it is the subject of a paper by J. A. Woolley and colleagues from three divisions of the 3M Co., St. Paul, Minn. They, too, found that only those packaging materials opposite and adjacent to the active surface of a die affected it with their alpha emissions. Those parallel with it had the biggest effect.

As in the Coors Ceramic paper, they concluded that with careful selection of raw materials, it should be possible to formulate conventional 90–95% alumina ceramic semiconductor packaging components with alpha fluxes of about $0.1~\alpha/\text{cm}^2/\text{hour}$ and glass package sealants with alpha fluxes of about $0.5~\alpha/\text{cm}^2/\text{hour}$. Also 99.9% alumina ceramic semiconductor packaging components with alpha fluxes in the range of $0.01~\text{to}~0.03~\alpha/\text{cm}^2/\text{hour}$ are possible, while anything lower than $0.01-\alpha/\text{cm}^2/\text{hour}$ radiation will require raw materials with uranium and thorium contents lower than are currently available. To go below the 0.01~level, analytical techniques for separating and concentrating uranium and thorium will have to be combined with direct alpha flux measurement.

An alpha count actually at the 0.01 level is obtained by the author of a fourth paper from Semi-Alloys Inc. of Mount Vernon, N. Y. Samuel Levine did it by going to gold-plated metal lids that are used for hermetic sealing and gold-tin eutectic solder. He put a gold-plating salt, formulated from extremely high-purity gold, in an electrolytic bath containing a proprietary chelating agent. This agent prevented the thorium and uranium ions from plating out with the gold.

Porcelain-coated steel is one of the more exciting substrates to have come along in years, being relatively low-priced, strong yet bendable, a natural heat sink, and suitable for both printed-circuit and thick-film techniques [Electronics, March 15, 1979, p. 125]. Now it seems likely to add good performance at microwave frequencies to all its other virtues.

Porcelainized steel for high frequencies

In one of the key papers on substrate development, A. Schwarzmann of RCA's Government Systems division in Moorestown, N. J., shows that this type of substrate is a potential low-cost alternative to alumina substrates for high-frequency applications. RCA's investigation compared alumina with both commercial electronic-grade porcelain-coated steel and a special substrate, porcelain-coated copper and steel.

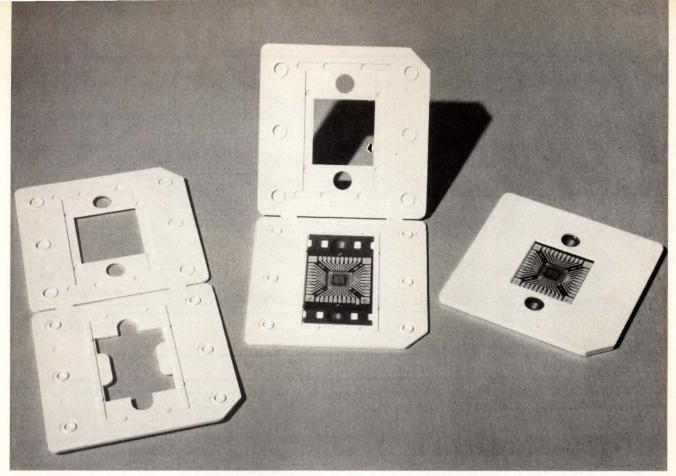
In one experiment, a thick-film copper conductor was screened onto each metal substrate to form a microstrip transmission line with a 50-ohm characteristic impedance. On the commercial steel version, it had an attenuation of 0.9 decibel per inch normalized to 1 gigahertz; on the copper and steel, attenuation was 0.34 dB/in. A thin-film chrome-gold equivalent on an alumina substrate yielded an attenuation of 0.28 dB/in. (see Table 2).

In the second experiment, a low-noise amplifier and a high-power transistor amplifier were constructed on a porcelainized metal and an alumina substrate. The low-noise amplifier was designed to operate from 800 to 1,300 MHz. On metal, it has a gain of 20 dB and a noise figure of 3 dB, only 0.2 dB higher than on alumina; all other parameters were about the same. The power amplifier on the metal substrate performed as well as the one on the ceramic substrate, with only 0.5-dB less gain but with the advantage of a lower junction temperature.

Fine lines for thick films

The screened-on circuit patterns of thick-film hybrids seldom achieve high yields for line widths much below 4 mils. But Yutaka Watanabe and his coauthors at Fujitsu Ltd. in Japan have obtained line widths down to 2 mils with a new method: they substitute photolithography with a water-soluble negative photoresist for the normal screening of thick-film materials through a steel mesh.

In the new technique, a thick-film paste is first printed over the entire substrate surface. Then the resist is coated over the dried thick film, exposed through a photomask, and its unexposed areas washed away with water. Next, an organic solvent is sprayed over the newly exposed thick film to dissolve it, leaving the desired circuit pattern. Finally, with the resist still in place, the substrate is heated to a predetermined temperature, firing the thick film and evaporating the resist. With this technology, a large hybrid has been built having 25 IC chips on a 30-millimeter-square (1.2-in.^2) substrate. In addition, this process creates resistors with a range of 10 ohms to 100 megohms, in contrast to the 10 Ω to 10 M Ω of conventional thick-film hybrid resistors.



3. Individual tape-automated bonding. Honeywell Information Systems has developed individual carriers for tape-automated bonding of chips to hybrid substrates. Shown here is a 35-mm expendable TAB carrier in open, partially folded, and closed positions.

Tape-automated bonding (TAB) is a means of mass-producing interconnections between chips and their packages; it uses IC interconnects (spiders) etched into a copper surface of a sprocketed nonconductive film. Usually, reel-to-reel handling moves the tape first through an automated bonder, where specially bumped chips are mass-bonded to the inner leads of the interconnects, then through a machine that bonds their outer leads to lead frames, which are then molded into plastic dual in-line packages. An equivalent system for hybrid manufacture must perforce be more complicated since a single hybrid substrate must often hold as many as 50 different device types.

Automating hybrid assembly

John Kowalski, manager of advanced equipment engineering at Honeywell Information Systems, Phoenix, Ariz., describes one solution in his ECC paper (for other solutions, see *Electronics*, Sept. 28, 1978, p. 120). Kowalski's procedure is to cut up a reel of tape after the chips have been bonded to it, store each piece in a carrier in an interim magazine, test them, and then unload carriers from assorted interim magazines into a final magazine, which thus contains the assortment of chips needed for a given hybrid.

At Honeywell, a framer cuts up the film and loads the frames into the carriers (Fig. 3). A sequencer stores these carriers and loads their contents upon demand into the final magazine. A placement unit accepts the final magazine, excises chip-plus-interconnect from its piece of film, forms the leads, and places it in the hybrid

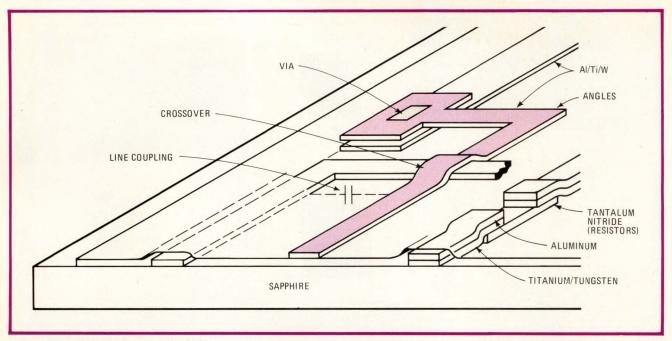
assembly. A reflow unit then reflow-solders the two together. Since it is expensive to stock reels of different devices, Honeywell is looking into extending the carrier concept to the inner-lead bonding of each chip to individual frames of tape.

Some hybrid attractions

Among the more interesting hybrids discussed at ECC this year are a nonvolatile solid-state relay, an inductor, a substitute transformer, a high-voltage yet mass-producible SCR, and two GaAs MES FET developments.

The relay uses a p-channel metal-nitride oxide semiconductor (MNOS) transistor to remember its on or off state during power outages. Described by John A. Skok of Lockheed Missiles and Space Co., Sunnyvale, Calif., it is the functional (and more reliable) equivalent of a latching electromechanical relay. Besides the MNOS device, the hybrid package consists of a custom reset-set IC driven by a dual voltage-controlled current source through two optically coupled isolators.

Japan is the source of the solid-state inductor—or more precisely, a hybrid IC gyrator functioning as one. According to M. Nakamura of the Hiroshima Institute of Technology and his two coauthors from Tokyo and Hyogo, the phase delay inherent in conventional gyrators creates a problem in this application, for it causes instability in high values of Q at high frequencies. They therefore connect a phase-compensating capacitor to their IC gyrator, which has a maximum obtainable Q of about 100. Moreover, the temperature coefficient of the equivalent inductance was observed around 200 ppm/°C



4. Sapphire substrate. High-density, high-impedance transmission lines can be designed on a supporting structure of sapphire. The drawing shows a two-level signal interconnect with thin-film resistors for impedance matching. Line widths are 5 to 10 micrometers.

at 2 MHz and below. In its hybrid IC form, the gyrator circuit has mini-mold transistors and chip resistors reflow-soldered on both sides of a ceramic substrate.

Another optoisolator circuit from Japan replaces the transformer in transmission systems and indeed is superior to it, say Y. Fukui and S. Yoneda of Tottori and Osaka Prefecture Universities. Their optoelectronic transmission device is very simple, being composed of two optoisolators in a positive feedback arrangement that yields a loop gain of less than unity. The experimental circuit can exhibit not only transmission gain or attenuation like that of a step-up or step-down transformer but also (under certain conditions) bilateral transmission.

Additionally, the device's input impedance is nearly independent of the external load impedance, making it ideal for suppressing impedance variation in a two-wire line. When optoisolators with a cutoff frequency of several kilohertz are employed, the device works at frequencies up to a few hundred kilohertz.

Making it better

Noteworthy for their efficiency at switching voltages of 1,400 and 2,500 volts are a pair of asymmetrical silicon controlled rectifiers (ASCRs) described by J. Y. Fichot and two colleagues from General Electric Co. in Syracuse, N. Y. The secret is a low-concentration diffusion process that should be far better than epitaxial deposition at producing large-area devices like these ASCRs on a volume basis, for it forms an n⁺ layer with fewer defects, less difficulty, and at lower cost. This n⁺ layer is inserted between the n⁻ bulk base and p⁺ anode of a conventional SCR to supply the p-i-n punch-through function. The resulting ASCR requires a much narrower n base width than an SCR for the same blocking capability—hence its switching efficiency.

Another processing breakthrough is described in a

paper on gallium-arsenide metal-semiconductor field-effect transistors. Lynn Kuller of the Rochester Institute of Technology of Rochester, N. Y., and James J. Whalen of State University of New York at Buffalo, recommend processing GaAs MES FETs as individual dice, typically 2.5 mm square, rather than by the wafer, when limited quantities are needed. Material cost per project is reduced because photomask requirements are relaxed: the entire set of masks for one die can be shrunk 400 times onto a plate little more than 4 inches square.

The procedures developed were used to put four different GaAs MES FETs on a single die. All had 6-µm gate lengths and each had a different pinchoff voltage for possible application in multivalued logic gates. Variable pinchoffs would not be possible if full wafers were fabricated and subsequently diced up.

High-impedance hybrid for gigahertz logic

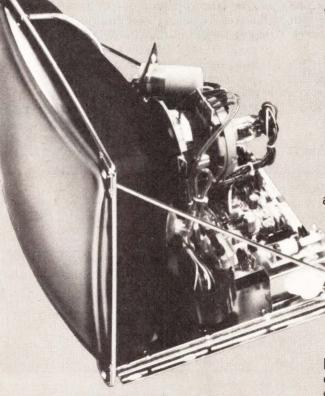
Integrated arrays of GaAs MES FETs switch much faster than currently available emitter-coupled logic—in 50 to 100 picoseconds, rather than 200 to 400 ps. But the output impedance of large integrated GaAs arrays is inherently high, so that the characteristic impedance of supporting transmission structure must be high to minimize signal attenuation between chips. (In general, a high-impedance transmission structure is advantageous for any high-speed circuit family because it reduces the amount of power required for signal transmission between devices.)

Edward Lewis of Raytheon Co.'s Missile Systems division in Bedford, Mass., describes a fine-line, hybrid technology that meets these goals. It centers on a two-level structure of 5- μ m-wide lines on a sapphire substrate. Using projection lithography, thin films of resistive material and aluminum were evaporated onto the sapphire. A charactistic impedance of 100 to 300 ohms can theoretically be achieved (Fig. 4).

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Circle 117 on reader service card

Designer's casebook.

Up/down counter processes data over single channel

by N. Bhaskara Rao U. V. C. E., Department of Electrical Engineering, Bangalore, India

Two inputs are normally required for incrementing and decrementing an up/down counter—a count-up command line and a count-down line. But commands can be sent and received over a single channel if they are first multiplexed. Shown here is a transmitter-receiver pair for the one-channel system, which is particularly cost-effective over long distances.

At the sending end, it can be seen that $\bar{x} = QU + \bar{Q}D$, where x represents the transmitted signal, U is the count-up variable, and D is the count-down variable. It is assumed that the width of the U and D pulses is not more than a few hundred nanoseconds, and that the frequencies of U and D are relatively low.

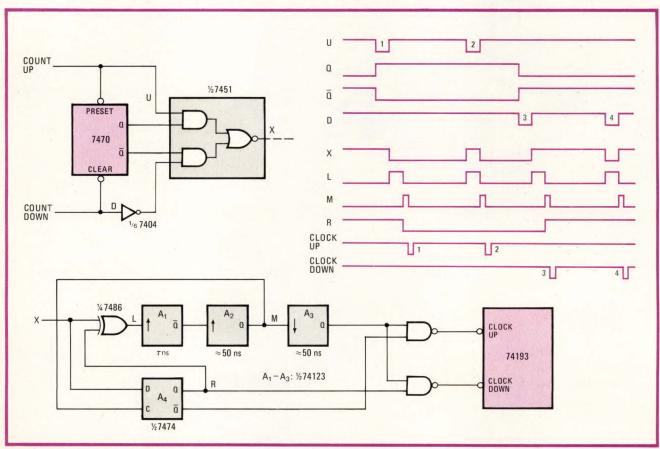
When negative-going count-up pulses appear on the U

line, the 7470 flip-flop is preset to Q=1 and so $x=\overline{U}$ thereafter. Thus x moves from logic 1 to logic 0 on the trailing edge of the count-up command.

Similarly, a count-down command clears the 7470 and so x = D. Thus x moves from logic 0 to logic 1 on the trailing edge of the down command. The timing diagram details transmitter operation.

The receiver determines if variations in x are due to changes in U or D by using an indirect and inexpensive phase-locking scheme. Transitions in x are introduced at the input of the 7486 exclusive-OR gate. Feedback loop A_1 , A_2 , and A_4 acts to bring point L high, regardless of whether the transition is positive- or negative-going. One-shot A_1 , having a set delay time, τ , slightly greater than the width of the U and D command pulses at the transmitter, then triggers one-shot A_2 . By this time, x has stabilized, so that a logic 0 (U pulse) or a logic 1 (D pulse) is clocked into A_4 , thus bringing point L low τ nanoseconds after it goes high.

Meanwhile, one-shot A_3 is fired, and the active contents of A_4 are transferred to either the clock-up or the clock-down port of the 74193. The receiver's timing diagram should be inspected to clarify operation.



Self-synchronous. Flip-flop and gates pack count-up and count-down commands on a single data line for transmission over long distances (top). Receiver (bottom) senses polarity of pulses, without using complicated synchronous detectors, to increment or decrement up/down counter. Three one-shots provide superior operation as compared to detection schemes employing sequential logic.

Annunciator control uses only passive components

by John A. Haase Fort Collins, Colo.

Combining relays with other passive components, this circuit provides time delays of anywhere from milliseconds to minutes without the need for the polarizing potentials normally required by monostable multivibrators. Such an electromechanical arrangement is ideally suited to the implementation of a practical call controller, or annunciator.

Delays are produced by first generating a staircase voltage. Pushing button PB_1 momentarily latches relay K_1 and energizes its bell circuit. The bridge circuit used with each relay permits the use of an inexpensive dc relay.

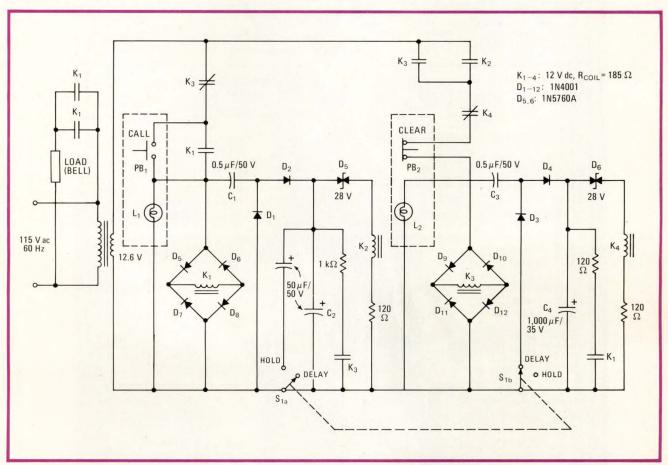
Call-indicator lamp L_1 then lights, and supply voltage is applied to C_1 , C_2 , D_1 , and D_2 , which make up the staircase generator. The step interval of the rising output voltage, V, at the junction of D_2 and C_2 becomes $\Delta V_o = C_1 E(10^3)/C_2$ millivolts per cycle, where E = 12.6(1.414) = 18 volts. Note that the diodes are consid-

ered passive elements in this application, as their characateristic curve, per se, is not utilized in the generation of the staircase waveform.

Circuit constants are selected so that D_5 , which serves as a comparator, breaks down after 155 cycles (2 seconds), when output voltage V reaches 28 v. Relay K_2 is then energized, enabling K_3 to close and lamp L_2 to light, because the alternating voltage is applied to a second delay circuit through one of the normally open contacts of K_2 . At the same time, voltage to relay K_1 is removed, since the normally closed relay contact of K_3 (in K_1 's energizing path) opens. Simultaneously, C_2 is discharged by K_3 's closed relay contact (in series with the 1-kilohm resistor).

Relay K_3 remains closed for 80 seconds to prevent repeated (and most times annoying) calls. At that time, the output voltage across C_4 , generated by the second staircase waveform, steps to 28, whereupon D_6 breaks down and relay K_4 is energized. Relay K_3 then opens and the path of relay K_1 is reactivated to accommodate call requests, while C_4 discharges.

Call requests may be extended to 4 seconds by placing switch S_1 in the hold position. In this mode, relay K_4 does not come into play, so the user must wait an infinite inhibiting time before initiating a second call request. Under this condition, push button PB_2 must be depressed to clear the circuit so that it can respond to calls.



Charged delay. Electromechanical relays and other passive components form charge pump that generates a time-dependent staircase voltage, V, for call controller. By suitably selecting diodes D_5 and D_6 so that their breakdown voltages conform to some preset value of V, the circuit provides delay. Depressing PB₁ rings bell for 2 seconds, inhibits circuit for 80 seconds to prevent quick second requests.

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LEDs track signal level in visual data monitor

by Michael O. Paiva Teledyne Semiconductor, Mountain View, Calif.

In this circuit, a matrix of light-emitting diodes is combined with an analog-to-digital converter and multiplexing logic to form a dual-setpoint meter. The LEDs are used to track changes in the input data and display the setpoints. The unit may be considered a variation of the analog panel meter; it will find many uses in industrial control applications where it is necessary to observe quick changes while determining whether data is within a preset range. By adding a dual comparator to the circuit, an alarm can be sounded when the input level goes outside the range.

The signal to be tracked, V_{in} , and the upper and lower setpoint voltages are applied to an eight-channel multiplexer, A_1 . The a-d converter, A_2 , samples channel 1 first. After the conversion, pin 23 of A_2 goes high and

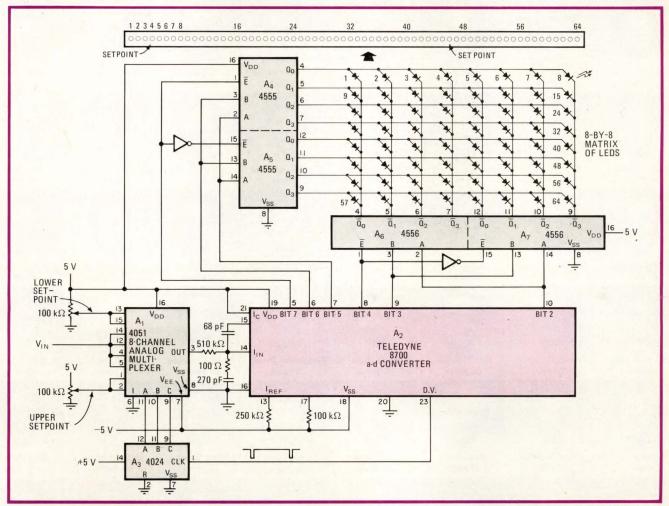
advances the binary counter, A_3 . A_3 then addresses the second channel of the multiplexer, and so on, until each channel is scanned in sequence.

Bits 2 through 8 of the a-d converter, representing the binary equivalent of the voltage sampled, drive A_4 - A_7 , which are wired as two one-of-eight decoders. Thus each voltage is converted into a control signal that drives one diode in the eight-by-eight-diode matrix.

The setpoint voltages are sampled twice during each scan cycle (each is connected to two input channels), while the input signal, $V_{\rm in}$, is connected to four channels and so is scanned four times per cycle. Thus the brightness of the LED corresponding to $V_{\rm in}$ is twice that of the setpoint LEDs, making it easy to differentiate between the three signals.

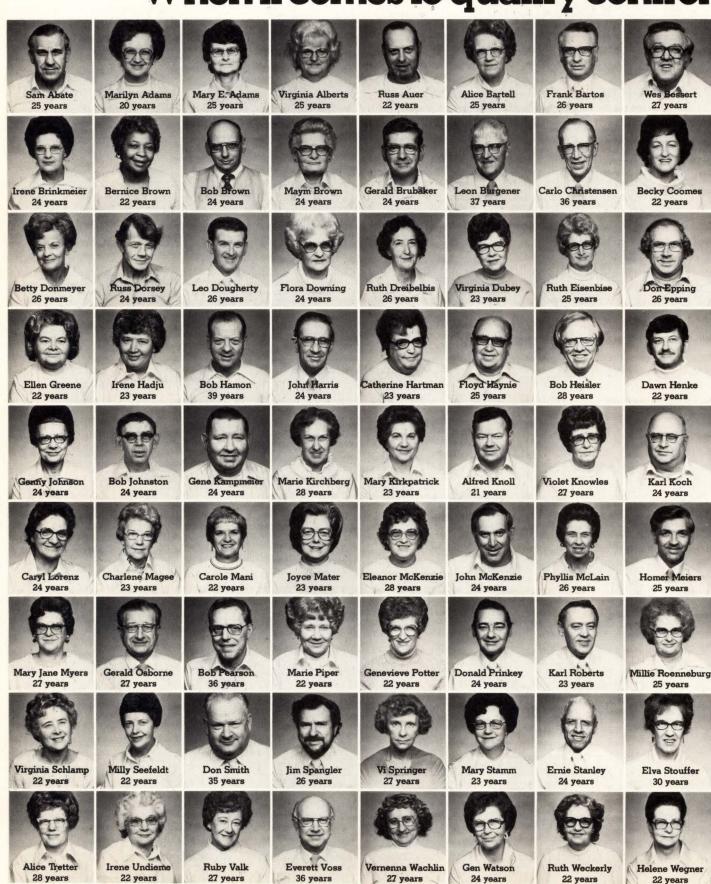
The circuit's worst-case response time is two scan cycles. A_2 has a conversion time of 1 millisecond, so that the display will require 2 ms to follow a change in V_{in} and 4 ms to follow any change in the setpoint potentials. Because of this high refresh rate, no flicker will be observed on the LED display.

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay \$50 for each item published.



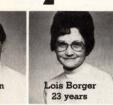
Visualizing voltage. Eight-by-eight-LED matrix and C-MOS logic form analog dual-setpoint meter. Setpoint potentials and data voltage V_{in} are each introduced into multiplexer and scanned in sequence, then converted into control signals that light the appropriate LEDs in the matrix. Setpoint LEDs are half the brightness of the LED representing V_{in} because they are sampled at half the rate.

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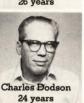




26 years











25 years



39 years







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24 years













22 years



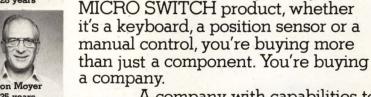






















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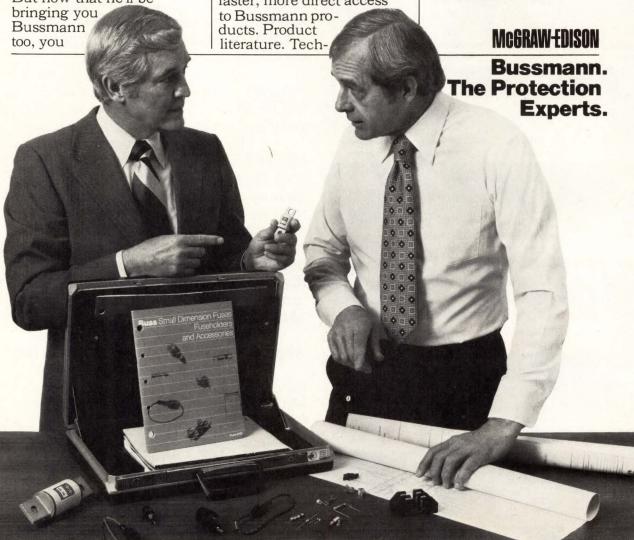
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The race heats up in fast static RAMs

While Fairchild's bipolar parts and Intel's MOS chips slug it out in the sub-55-ns arena for random-access memories, other manufacturers are gearing up their processes too

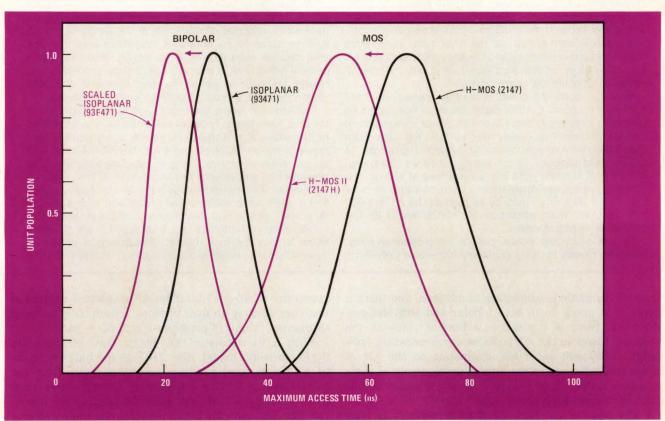
by Raymond P. Capece, Solid State Editor

☐ Memory system designers have a lot to look forward to in very high-speed semiconductor random-access memories. Over the next 12 months, static RAMs with access times of 55 nanoseconds or less will proliferate, as chip manufacturers scramble for secure positions in the sockets of their biggest customers, the builders of minicomputers and mainframes. For customers, that is good news: it means a price war that will drive down the cost of fast static memory.

Serving as high-speed buffers and cache memories, this portion of the RAM spectrum will see bipolar designs fighting against the encroaching metal-oxide-semiconductor chips. At the moment, there are two chief contenders: Fairchild on the bipolar side and Intel on the MOS side. Both companies are poised and ready to strike

with new processes (Fig. 1); but not far behind are such companies as Motorola, Advanced Micro Devices, Signetics, National, Mostek, EMM Semi, American Microsystems, and Texas Instruments.

It is prophesied that the world of memory systems will inevitably be all MOS, because these parts ultimately will be cheaper to build and they consume less power. However, that prophecy may not hold, for the commitment to a device type, as always, will take into account considerations other than technology. Delivery schedules and the availability of a second source will often take priority over price and even performance. Of course, designers must keep track of what is on the market and what is coming. (The table on p. 132 will serve as a handy reference for the present and future parts.) The



1. **Downward bound.** Curves for access-time distributions of the leading bipolar and MOS 4-K static RAMs tell the story: both are getting faster. Intel and Fairchild have begun production using processes (color) that will pare access times by 10 to 20 nanoseconds.

Watch out for Super C-MOS

Static random-access memories made with complementary-metal-oxide-semiconductor processes tempt memory system designers with their attraction of one tenth the power dissipation of n-channel MOS parts—although traditionally they lag a generation behind n-MOS static RAMs in speed and only somewhat less in density. Still, C-MOS adds low, low power consumption to the list of price, performance, and availability tradeoffs between bipolar and n-channel MOS chips.

C-MOS static memories are, at the very least, displacing n-MOS in moderate-speed applications where power is a strong consideration. Moreover, the development over the past few years of high-performance processes is starting to pay off in the high-speed arena as well.

First production. The magic access time of 55 nanoseconds has been reached by several manufacturers working with advanced self-aligned and oxide-isolated C-MOS processes. But the first to get there with a production part is Japan's Hitachi Ltd., which is surrounding an n-channel memory array with C-MOS peripheral chips to get high speed and low power. It has dubbed its 4,096-by-1-bit RAM the 6147, and its goal is clear: the part is a plug-in replacement for Intel's industry-standard 2147.

The 6147, shown to the right, is an impressive part. Built with a 3-micrometer process the Tokyo-based firm calls Hi-C-MOS, it employs several design twists, such as the use of both p- and n-type wells and the incorporation of bipolar transistors as output drivers. One U. S. C-MOS manufacturer who got a peek inside found "extremely innovative processing and design."

At 17,000 mil², its die is significantly smaller than Intel's 25,000-mil² 2147. Moreover, the part carries a 55-ns maximum address-access time and an absolute maximum chip-select access time of 55 ns—it pays no penalty for a short deselection period as the Intel part does. Most impressive are its worst-case standby power dissipations: 4.2 milliwatts in the standard version and only 520 microwatts in a selected low-power version.

However, operating power is another matter: the 6147 exhibits the typical C-MOS dependency of dissipation on operating frequency. The maximum power dissipation of the device cannot be clearly inferred from the data-sheet specifications. Average operating current is given as 14 milliamperes typically, which translates into a dissipation of 73.5 mW, but that spec is at a cycle time of 150 ns. The absolute worst-case dissipation is likely to climb to more than half a watt and could be as high as the 2174's 900 mW. Still, the main attraction of C-MOS lies in its low dissipation during standby.

To get such low power out of its n-channel array, however, Hitachi is using extremely high-value polysilicon

loads—the phosphorus-doped resistors are on the astronomical order of 40 gigohms. Since static RAMs with polysilicon load resistors of even far lower resistance have fallen prey to soft errors caused by alpha-particle radiation [*Electronics*, March 15, 1979, p. 85], the 6147 should be besieged by soft errors.

Not so, says Hitachi, claiming no soft errors until the supply voltage is reduced to about 1½ volts. It offers as an explanation the unique construction of the chip: the n-type transistors of the memory array sit in a grounded p well sunk into an n-type substrate tied to the positive supply. That electric field sweeps away the memory-disturbing charge carriers that alpha particles generate. So confident is Hitachi that it will begin offering third-quarter samples of its 16,384-by-1-bit static, a scaled-down extension of the 6147 design.

The alpha-particle invasion of standard n-channel static RAMs may swing more attention to C-MOS statics than anything else. C-MOS may offer low power dissipation without any increased susceptibility to alpha particles, whereas n-channel devices become more susceptible as their power is reduced. Look at the differing approaches to power reduction, says James A. Ford, manager of very large-scale integrated design for Control Data Corp.'s Digital Image Systems division, Minneapolis.

Susceptible. "Power is reduced in n-channel devices by using very low GM [transconductance] load devices or by using extremely high-value load resistors," he says. "In either case, the memory cell is inherently susceptible to flipping when an alpha-induced current is injected into the off side of the cell.

"In the case of C-MOS technology, power is reduced by an off transistor in series with an on transistor. The on transistor's effective resistance is in the range of 2 to 5 kilohms, three to six orders of magnitude less than the load devices used in n-MOS memories. When an alpha particle hits a C-MOS memory cell, the current induced is readily sourced or sinked by the device in the low-resistance state, without upsetting the state of the cell."

Perhaps that is why the major C-MOS manufacturers in the U. S. have begun to apply the tricks used by n-channel MOS makers. For example, Harris Corp., Melbourne, Fla., currently makes 1,024-bit and 4-K C-MOS RAMs that, with access times of several hundred nanoseconds, are sold primarily into applications needing extremely low power.

However, as long as two years ago the company identified a need for combined low power and high speed—both its military and mainframe customers want this combination of attributes in a RAM—and it will definitely make a play for that market. According to James F. Townsend, advanced product planner, Harris's C-MOS

name of the game is technological advance, and there is plenty of it going on in both bipolar and MOS designs. Moreover, there is a whole new host of chips on the horizon, thanks to the advances in complementary-MOS design. They add super-low dissipation to the list of design tradeoffs, and recent intense development of these processes is starting to pay off in terms of higher speeds (see "Watch out for Super C-MOS," above).

Focal point of the high-speed RAM industry is Intel Corp's 2147, announced in July 1977. It is no secret that every manufacturer aiming at high-speed MOS memories

covets this 4,096-by-1-bit chip. Although half a dozen of them are working on their versions, only Intel is shipping substantial volume of premium-speed, 55-ns parts.

With a six-transistor cell design (two of them are depletion-mode loads), the 2147 is an industry standard—the pin configuration received approval from the Joint Electron Device Engineering Council more than three years ago—and is in great demand. Other manufacturers undoubtedly began planning their parts as long ago as did Intel. But they are finding it a tough one, chiefly in the processing but also in design and layout

process is in its fifth generation, each having added a process variation that offered some improvement in speed or density. "We're closing the gap on n-MOS manufacturers in speed just as they are on bipolar makers," Townsend says.

He would not detail the process enhancements, but it is a good bet they are like those that other C-MOS manufacturers are beginning to use. Aside from shrinking the layout rules from the conservative 4 to 41/2 micrometers, companies like American Microsystems Inc. and Intersil Inc., both in Cupertino, Calif.; Motorola Inc.'s Semiconductor Group; Solid State Systems Inc., Montgomeryville, Pa.; and others are using self-aligned processes and localoxidation techniques to reduce the capacitance that hinders speed in C-MOS.

Faster. Harris has reportedly offered samples of 1-K RAMs with maximum access times of 50 ns without fully exploring design-rule shrinkage—at about $3^{1/2} \mu m$, the process is comparable to Intel's H-MOS. Indeed, it is likely that in 1980 sub-100-ns C-MOS RAMs will be readily

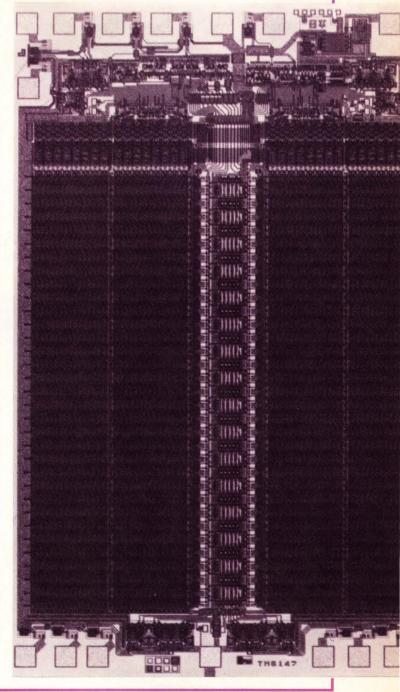
available from several manufacturers.

Yet another C-MOS approach comes from RCA Corp.'s Solid State division in Somerville, N. J., and Rockwell International Corp.'s Electronic Devices division in Anaheim, Calif. They are developing memories using silicon on sapphire. Although RCA's parts are showing density advantages-its 4-K RAM is 24,000 mil², as against Harris's 30,000-plus—the parts are not yet yielding the speed that SOS promises. However, the company will make the most of the density advantage, having already unveiled designs for its 16-K static RAM at conferences earlier this year.

Toshiba Corp., with increasingly strong sales of 1-K and 4-K C-MOS RAMs in the U.S., is readying a 2-K-by-8-bit part for midyear samples that will use a 3-µm process. Moreover, the Tokyo firm has its eye on the high-speed business with its C-MOS-on-sapphire process. A 4-K chip in the laboratories is running at a remarkable 40-ns access time, and it could be a predecessor of SOS parts for buffer

and cache memories sometime next year.

C-MOS manufacturers expect that their parts will always cost more, though a premium of 20% to 30% is one they would accept comfortably. To be truly competitive with n-channel MOS, they will have to pare down die sizes more. Harris and RCA feel that the 2-µm geometries available in 1981-82 would give C-MOS substantially the same size as n-MOS-in parts such as static RAMs and random-logic devices, which can take advantage of C-MOS's inherently smaller implementations of functions like transmission and exclusive-OR gates. "We mainly have to tighten up our layouts," says Harris's Townsend.



(see "MOS: not so simple now," p. 129).

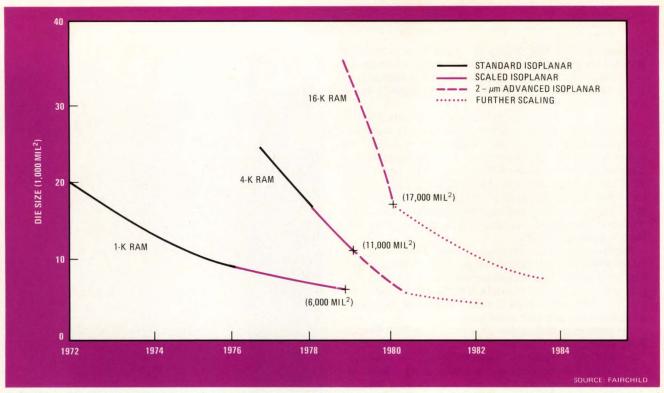
Now Intel has announced the 2147H, with worst-case access times of 35 and 45 ns [Electronics, March 1, 1979 p. 156]. Could the Santa Clara, Calif., manufacturer really be that far ahead of so many other respected static RAM builders who have not yet achieved 55-ns devices?

Deliveries alone will tell. To build the 2147H, Intel has parlayed its high-performance H-MOS n-channel process into H-MOS II by thinning gate oxides to 400 angstroms, scaling channel lengths from 31/2 to 2 micrometers, and tightening up its process. The company is

counting on direct step-on-wafer projection lithography equipment just coming on line, for the DSW units are the only machines capable of 2-µm resolution in production.

Of course, Intel is a double threat in the computer memory market, as it is the originator of the 1,024by-4-bit 2114, which offers access times ranging from 100 to 400 ns. Widely imitated by other chip makers, the 2114 has almost reached the status of a jelly-bean part.

But, it is the fine lines claimed for the 2147H that concern Fairchild Camera and Instrument Corp., the bipolar RAM pioneer on whose toes Intel is stepping. "If



2. Evolving. Fairchild is reducing die sizes of bipolar memories with its Scaled Isoplanar process, which puts 3-to-3½-µm lines in place of 4½-µm lines. The first redesign will bring the 1-K RAM down to 6,000 mil² from 9,000 mil² and the 4-K RAM from 17,000 mil² to 11,000 mil².

they are really at 2 μ m, that puts them several years ahead of everyone else," says Stephen Jasper, group marketing manager for bipolar large-scale integrated circuits at the Mountain View, Calif., Company.

Jasper's job is to chart a course for Fairchild's transistor-transistor-logic RAM products, which include the industry-standard 1-K-by-1-bit 93415 introduced in 1973 (and the popular three-state-output version, the 93425) and the 4-K-by-1-bit 93471 rival to the 2147 but with a different pinout. "I've got to plan on H-MOS II being a production reality within 12 months," he says.

In fact, he had better expect the worst, according to Kirk McKenzie, director of memory marketing at Intel's Aloha, Ore., division. "We're offering samples of the 2147H now and will be in volume production by the third quarter," he says. The part has a premium access time of 35 ns (compared with the 93471's 45 ns), as well as offering a power-down mode that retains data while cutting power dissipation by 80%.

Moreover, H-MOS II is making possible the recent 1-K 2115H, whose worst-case access time of 20 ns upstages the 30-ns 93415A from Fairchild, with which it is plug-compatible. Next to arrive, adds McKenzie, will be a high-speed, 16,384-by-1-bit static RAM, probably some time in 1980.

However, Fairchild is ready to counter with a taste of the medicine that MOS makers use: the shrink (Fig. 2). "The 93415A out today is built with conservative, 4-\mu lines," Jasper says, "and we've already shrunk that to a geometry comparable to MOS." Using the company's new Scaled Isoplanar process for 3-\mu m lines, the 93F415 reduces the 9,000-square-mil die of the 93415A to only 6,000 square mils. A general introduction should come

late in the second quarter of this year, offering a part with a worst-case access time of 20 ns.

Fairchild also has plans on the 4-K-by-1 front. There will be a 93F471 that will drop the 17,000-mil² die of the 93471 down to 13,000 mil². "We expect the shrinks to pare down access time to well below 20 ns in a year or so," Jasper says.

The firm has other parts up its sleeve, involving its coming DSW lithography equipment. This is the same half-million-dollar system from GCA Corp. that is giving Intel its 2-\mu m parts. So Jasper offers the 1980 possibility of a 4-K RAM the size of present 1-K parts and a 35-ns 16-K-by-1 chip with a die size less than 20,000 mil².

Process differences

One point in favor of bipolar parts, as Fig. 1 shows, is that processing yields parts of uniform speed, unlike the wide range of speed distribution exhibited by MOS processing. The speed of bipolar circuits depends on relatively easily controlled diffusion steps, whereas MOS speed is extremely dependent on lithographic registration. "When a bipolar part is specified at 30 ns, all dice on the wafer are 30 ns," Jasper says.

Of course, power dissipation can be bipolar's Achilles heel. For example, one major computer firm has all but pronounced Fairchild's 1-K 93415 dead because Intel's MOS 2115 does the same job at less power. However, Jasper argues that in many cases pushing MOS to high speeds kills its power advantage: at the 4-K level, Intel's 2147H dissipates 945 milliwatts, compared with the Fairchild 93471's 892.5 mw.

Moreover, Fairchild is in volume production of the 93L415, which drops dissipation from 814 to 182.5 mw,

MOS-not so simple now

Lest MOS manufacturers continue to sell their high-speed random-access memories against bipolar RAMs with the old pitch, "The process is simpler, the part will eventually cost less," let the buyer beware. High-speed metal-oxide-semiconductor RAMs are built with processes that could easily take as many steps as bipolar chips, and the yield of good chips and the speed distribution of the dice on each wafer depend directly on the ability of the manufacturer to keep each of those mask steps aligned.

Moreover, the 2-micrometer channel lengths in Intel's latest H-MOS II methods and to come next year from other MOS makers put a strain on the process. All but extinct will be any advantage over bipolar processing, considered more complex because of the two semiconductor types, the epitaxial construction, and the oxide isolation.

"People still think MOS is cheap from the old four-mask p-channel days," says Frank Barone, National's director of bipolar memories. "Even our emitter-coupled-logic process is simpler, and we're betting that one day the costs for all high-speed memories will be equal."

Though he acknowledges that the scene is changing, Steve Jasper, group marketing manager for bipolar LSI at Fairchild, still puts bipolar at a 2:1 speed advantage, while giving MOS memories a cost edge. "It's the distribution game they're playing," he says, referring to the wide range of speeds that any MOS run yields. "The center of their distribution curve is what you have to look at."

More steps. The basic n-channel polysilicon MOS process requires five masking steps: field oxide, polysilicon, contacts, metalization, and pads. Moving to a higher density adds another mask step for buried contacts, and to get the threshold for a depletion-mode load transistor, another mask is needed.

Moreover, each time a device with a different threshold is added, that is another mask step. For example, a high-performance memory chip might use two types of depletion-mode transistors: those in the memory array would be lower-power devices with a threshold of $-1\ \text{volt},$ whereas output transistors would get a -3-V threshold for

more current drive. Similarly, enhancement-mode transistors with several thresholds can be advantageous in high-speed designs. Before long, the simple MOS process is using 10 masks—as many as bipolar.

Also, scaling down to $2^{1/2}~\mu m$ or less cuts into yields. Arsenic dopants must be used, and that means ion implantation with a very high-energy beam that will heat up the wafers and could even crack them; thus special cooling precautions must be taken.

Resistance. Finally, there are circuit-design considerations. The resistance of polysilicon becomes a problem, because the RC time constant of the circuit can hold back the speed of a memory part. Designing around that resistivity is tricky and requires juggling chip layout.

Since the number of good dice per wafer is still the best measure of cost, keeping die size as small as possible remains the name of the game. There, bipolar parts are showing an advantage.

In the latest version of Fairchild's 1-K static bipolar RAM, the geometries have been reduced from conservative $4^{1/2}$ - μ m lines to the resolution of present-day high-performance MOS—about $3^{1/2}$ μ m. That makes the 93F415 a 6,000-square-mil die. By comparison, even Intel's equivalent MOS 2115H, which uses 2- μ m channel lengths, will yield a die greater than 10,000 mil². Moreover, in 1980, Fairchild will apply 2- μ m geometries that will reduce its 4-K RAM to less than 10,000 mil².

A feeling throughout the semiconductor industry has long been that fast bipolar memories and dense MOS memories would clash when both processes were tried for a fast 4-K static RAM. Because only Fairchild and Intel are shipping the parts and neither has a dependable second source, there are not enough players yet to tell.

Meanwhile, Fairchild's Jasper is looking to jump back to the 1-K level and set a precedent with the shrunken 93F415: true cost competition for the first time between bipolar and MOS. "With a 6,000-mil² die, we ought to be able to attack the 2115 and get back some of that business we've lost," he says.

and the 93L471, which has a dissipation of 472.4 mW, Jasper says—but they are offered only with slower access times. Although the L parts are selected from standard production runs, the company is working hard on reducing power dissipation, as are other firms.

Fairchild acknowledges that a low-power standby feature is an advantage for MOS chips and a problem for bipolar parts. "The applications we see, however, are speed-oriented, and the users don't care," Jasper says. Still, others think the inherent power-down capability of MOS will be a boon, especially in applications with large arrays of statics (see "On powering down," p. 131).

Perhaps the greatest 4-K problem for Fairchild is the lack of a second source for the 93471. Jasper cites as a potential source Motorola, the only other manufacturer shipping the 93415A in volume. However, Motorola is not tipping its hand yet.

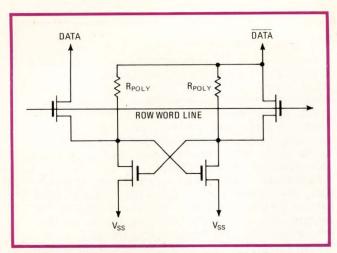
Yet Motorola will make Fairchild's emitter-coupled-logic 4-K memory, the 10470. Interestingly, all of Fairchild's transistor-transistor-logic memories start out as ECL parts; that is how the 93471 ended up with a nonstandard pinout, the company says. In fact, the levels

used within the memory arrays of the firm's bipolar chips are the same for both species. The input- and output-level translating circuits determine whether the parts are ECL- or TTL-compatible—and the ECL versions hit the street first. The firm thus offers a full complement of ECL parts, mask-programmable for compatibility with either the 10K or 100K families.

Of course, ECL's speed isolates it from MOS competition, and that feature may make many bipolar makers more interested in second-sourcing Fairchild's ECL parts than its TTL parts. As is Motorola, Signetics, National, and others are aiming at a strong ECL capability.

Another factor are Japanese firms, hungry for U.S. market niches, especially with parts they find useful for their own mainframe computers. So these firms are building—and exporting—more and more ECL and TTL parts that are in short supply from the U.S. makers. The key Japanese companies are Hitachi Corp., Fujitsu Ltd., and Nippon Electric Corp., all three offering plug-in replacements for the 93415.

Like Motorola, AMD, and Signetics, Fairchild is in the somewhat awkward position of interleaving strategies for



3. Different cell. Mostek Corp.'s 4801 1-K-by-8-bit RAM boasts a die size of less than 20,000-mil². One reason: Mostek hooks the loads to the data line, rather than to the positive supply. Eliminating the need for $V_{\rm cc}$ to run through each cell permits smaller dimensions.

bipolar and MOS statics. It is developing its high-performance MOS process and has seen the first passes of a 2147-type part. There still is much tightening of the process to be done, says George Urbani, manager of MOS marketing, and samples probably will not be available until early 1980.

Urbani acknowledges that Fairchild's 2147 part will be competing with its own 93471. "But everyone with an MOS process will be doing that part," he says. "There's a lot of money to be made on it." The company's next move in MOS statics will be to boost density to the 16-K level, but the part will be slow and organized as 2,048 by 8 bits for microprocessors. "Then we'll proceed with a fast 16-K-by-1 part," Urbani says.

Motorola in both races

Already making moderate-speed static RAMs (the popular 4-K 2114 in standard and low-power versions and its own 4-K-by-1 6641), the Austin, Texas, MOS memories operation of Motorola Inc.'s Semiconductor Group is working on a 2147 type. Dual designs were developed, one with polysilicon load resistors, the other with depletion-mode transistor loads. Motorola found the latter to show slightly better speed, so it will likely end up in the first production parts, which will come in at just under 20,000 mil². Samples should start appearing around midyear.

Once the high-speed process is nailed down, the unit will look at other chip sizes and organizations. The 2115 looks interesting, and building it would not be a backward step, says David Ford, marketing manager for MOS memories. "Many customers we talk to are using cache memories 1,000 words deep, and that means either a 2115 or a part with a by-4 or by-8 organization. We even get some calls for by-9 parts, since many computer people carry along the parity bit."

Ford says a 1-K-by-4 part is too small. A better possibility for his company, so heavily into the microprocessor business, is the 1-K-by-8 organization, since slower runs of a byte-wide part can be sold for microcomputer applications.

Perhaps somewhat further out is the 16-K-by-1 RAM that Intel has in the works. "It's just too hard to tell right now if caches will actually go to 16,000 words deep," Ford says. "There are a lot of advantages, since you can do much less pushing and pulling of data with a big cache. We'll be keeping an eye on the Intel part."

Motorola's bipolar memory operation in Mesa, Ariz., has long concentrated on emitter-coupled logic because the company's 10K family is a major commitment to this technology for high-speed logic. It offers a half dozen ECL statics, ranging from 16-bit to 1-K sizes with speeds between 15 and 30 ns.

With its recently introduced version of the bipolar 93415, the firm is seeing that there is money to be made in the TTL arena. Since Signetics suffered a production hiccup, Fairchild and Motorola are the only U.S. suppliers of the 1-K 93415.

But the 4-K TTL part is another matter. "We're not yet committing on the 93471," says Ron Lipinski, manager of bipolar marketing. It is likely that the plans of the MOS memory unit for the 2147 have something to do with the bipolar outfit's indecision. At any rate, Lipinski says, a 4-K TTL part would follow 4-K ECL design, "and we won't have that until 1980." Motorola will be calling that part the 10470, a variant on its own numbering system to accord with Fairchild's for the first time.

AMD looks to both

Like Motorola and Fairchild, Advanced Micro Devices Inc. has a foot in both MOS and bipolar camps. It has just seen first passes of its 2147-type part, which it is calling the 9147. Samples should be available within the next couple of months. The part, built with fairly conservative geometries to achieve its size of less than 17,000 mils², uses polysilicon-load cells, says Lowell Turriff, marketing manager for MOS RAMS.

The Sunnyvale, Calif., firm now makes a 2114 version (its 9114); the 4-K-by-1 9044, its version of Texas Instruments' 4044; and the 9244, a 4044 version without power-down. Not unlike its competition, AMD's game plan for static RAMs calls for a relatively slow 2-K-by-8 part aimed at microprocessors.

Next could be another 50-ns part. "If you're going after speed, the part to do is the 1-K-by-8," says Turriff, who is looking for these byte-wide fast parts to be a factor in control stores for computers. "We see the market clearly segmented: either 100-to-150-ns access times or 50 ns and below." The forthcoming high-speed 16-K-by-1 static memory could be the next workhorse after the 2147, "but Intel will have to prove its capability," he adds.

On the bipolar side, AMD does plan to second-source Fairchild's 1-K RAM. Samples of three parts will be ready by midyear, says Ralph Cognac, marketing manager for bipolar memories: the 93415 and the three-state 93425, both at the standard 45 ns; and the 93415A, running at 30 ns. Also in the works for end-of-the-year samples is a low-power version, the 93LS415.

The company has used a standard diffused Schottky TTL process to build smaller memories, but for the 93415 it is introducing a high-density, high-performance, oxide-isolated process it calls IMOX, for implanted oxide.

On powering down

With its 2147 random-access memory, Intel Corp. introduced automatic power-down, a feature that will be a major issue in the struggle between metal-oxide-semiconductor and bipolar RAMs. In less than one memory cycle after access ends, the 2147 reduces its 900-milliwatt power dissipation 80%, to 158 mW—while retaining data, of course. The reduction in overall power consumption could approach 85% in large memory arrays, says Intel.

Bipolar memories offer no such mode, although several manufacturers are working on the basic cell design. Their inherent low impedance and poor thermal noise immunity dim prospects of future power-down designs with much better than a one-third savings in power.

Though the scales may seem tipped in MOS's favor, the situation is not so simple. A memory that goes to sleep when not needed can cost in system speed. Moreover, it can even prove to be a disadvantage in certain situations and can be troublesome when designing systems.

For one, powering up a chip that is powered down takes more time than if it were not in standby. Therefore, the designer must look beyond the RAM's address-access time (t_{AA} in part a of the figure), which only specifies the time required for valid data to appear at the output once the signals on the address lines are stable. He must consider the chip-select access time (t_{ACS}), the time required for valid data to appear after the chip is selected.

Critical window. In many memory systems, the chip-select signal is part of the address information; an access time longer than the address-access time will hinder throughput. The data sheet's fine print tells the story: chip-select access time can be as much as 75 ns on a 55-ns 2147 if the part is activated within 55 ns of being deselected. That critical timing window (between deselect and select) must be greater than 55 ns, lest access time be extended. It is, in fact, a highly vulnerable feature of the 2147. A glitch on the chip-select line, for example, can stretch the access time and thus slow a computer cache, while being very difficult to detect.

Mostek Corp.'s 1,024-by-8-bit 4801 uses a different

ADDRESS
LINES
(A₀-A₉)

OUTPUT
DATA LINE

CHIP SELECT
INPUT (CS)

OUTPUT
DATA LINE

HIGH IMPEDANCE

(a)

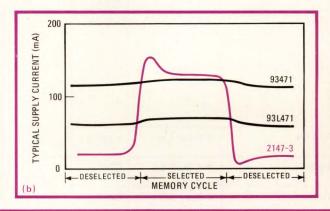
power-down scheme, and it is likely that others will appear as well. Mostek calls its technique address activation: within a memory cycle after the signals on the address line have settled, the part powers down. However, the 4801's standby power is only about 50% of the active power—not a tremendous reduction. On the other hand, the part's chip-select access time is that much better for it: 25 ns for the 55-ns version of the 4801.

Another argument against memory parts is that powerdown involves the noise generated by the switching transients as the many RAMs on a circuit board cycle through active and standby modes. As shown below in part b, the current through bipolar RAMs fluctuates by at most 10%, whereas MOS memories generate many transients as they switch through 10-to-1 current extremes.

Boards. Such signal behavior makes the job of laying out the memory boards for a high-speed cache difficult. Closer attention must be paid to board layout, conductor length and pattern, power-supply decoupling, and transient suppression. One mainframe designer likened the difficulties with power-down statics to those encountered when designing with hard-to-use dynamic RAMs.

The rule is that computer makers will always take the lower-power part—if it does not cost too much. Therefore, power-down may be here to stay if "memory system designers will go through the learning process for using power-down memories," as one component evaluator for a major computer firm puts it.

Still, critical cache memories must squeeze the most speed out of parts, and if they contribute little to a computer's total power dissipation, speed will easily take priority over power. As caches grow and as fast statics make their way into main memory, power dissipation will increase in importance. Even on its fast 6147P memory, Hitachi is offering power-down. The 6147P drops from a typical operating power of 75 mW (cycling at 150 ns) to a maximum standby of 4.2 mW. The Hitachi part, incidentally, suffers no extension in chip-select access time even with short chip-select intervals.



Cognac says the new process reduces transistor dimensions for faster, smaller chips.

AMD could use IMOX to build a 4-K bipolar device, but it is still in the throes of decision. "We're not committing beyond the 1-K density," Cognac says. Apparently, the MOS people at the firm are confident that they will be building a version of the competing 2147.

However, Cognac says there is plenty of life left in

bipolar RAMs. Not only can they be designed with better power-down features, but process improvements may lead to smaller chips and cost reductions. "Besides," he adds, "some markets, like the military, prefer to stick with the bipolar devices they have more confidence in."

Having built its MOS business on read-only memories, Signetics Corp. admits being a late starter on the RAM side of the technology. But the Sunnyvale, Calif, subsid-

THE STATIC RAM LINEUP							
Donat	Organization	Process	Maximum access time (ns)		Maximum power dissipation		Package
Part	Organization	type	Address access, t _{AA}	Chip-select access, t _{ACS}	Active (mW)	Standby (mW)	гаскаде
2115A/2125A	1 K by 1 bit	n-MOS	45 70	45 70	656	=	16-pin
2115AL/2125AL	1 K by 1 bit	n-MOS	45 70	45 70	394	_	16-pin
2115H/2125H	1 K by 1 bit	n-MOS	20 25 30	15 15 20	656 656 525	-	16-pin
93415A/93425A	1 K by 1 bit	bipolar (TTL)	45 60	35 45	814 814	-	16-pin
93L415/93L425	1 K by 1 bit	bipolar (TTL)	45 60	35 45	341 341	_	16-pin
93F415/93F425	1 K by 1 bit	bipolar (TTL)	20 35	15 20	656 656	-	16-pin
10415	1 K by 1 bit	bipolar (ECL)	20	7	780		16-pin
10422	256 by 4 bits	bipolar (ECL)	10	7	1,000	-	22-pin
10470	4 K by 1 bit	bipolar (ECL)	35	15	1,000	-	18-pin
93471A	4 K by 1 bit	bipolar (TTL)	45 60	35 45	893 893	-	18-pin nonstandard
93L471	4 K by 1 bit	bipolar (TTL)	45 60	35 45	472 472	_	18-pin nonstandard
93F471	4 K by 1 bit	bipolar (TTL)	30	20	893	-	18-pin nonstandard
2147	4 K by 1 bit	n-MOS	55 70	55* 70	900 800	158 105	18-pin standard
2147H	4 K by 1 bit	n-MOS	35 45	35* 45	945 945	158 158	18-pin standard
HM6147P	4 K by 1 bit	C-MOS	55 70	55 70	75**	4.2	18-pin standard
HM6147LP	4 K by 1 bit	C-MOS	55 70	55 70	75**	0.53	18-pin standard
MK4801	1 K by 8 bits	n-MOS	55 70 90	25 35 45	656 656 656	325 325 325	24-pin standard
μPD421D	1 K by 8 bits	n-MOS	85	85**	788	105	22-pin standard

^{*}chip-select access time may increase 10 to 15 ns if device is selected within a time equivalent to t_{AA} after deselection. **typical power dissipation at 150-ns memory cycle rate, 50% duty cycle. †2Q = second quarter.

Manufacturer and availability	Comments			
Intel, now	• no second source • plug-compatible with 93415/93425			
Intel, now	• 2115 has open-collector outputs • 2125 has three-state outputs			
Intel, 20 [†] '79	• built with HMOS II			
Fairchild, now Motorola, now Hitachi, now Fujitsu, now NEC, now Signetics, 2Q '79 AMD, 2Q '79	•93415 has open-collector outputs •93425 has three-state outputs •93415 equivalents: Fujitsu: MB7061 NEC: µPB2205D Hitachi: HM2510			
Fairchild, now Signetics, 30 '79	• low-power selection			
Fairchild, 2Q '79	high-speed version built with Scaled Isoplanar Process			
Fairchild, now Motorola, now Signetics, 20 '79				
Fujitsu, now Fairchild, now Motorola, 4Q '79 National, now	• 100 K logic family compatibility is available • Fujitsu equivalent is MB7072			
Fairchild, now Motorola, 1Q '80 Fujitsu, 2Q '79				
Fairchild, now	• no second source			
Fairchild, now	• low-power version			
Fairchild, samples 30 '79	 high-speed version built with Scaled Isoplanar Process 			
Intel, now AMI National TI AMD Motorola NEC Signetics Mostek	some manufacturers, preliminary data sheets quote lower power dissipation device powers down after chipselect goes high			
Intel, samples 20 '79	high-speed version built HMOS II			
Hitachi, samples now	•equivalent to 2147 at much lower power			
Hitachi, samples now	• low-power version of 6147P			
Mostek, samples now	 no second source pinout is ROM or PROM compatible device powers down after address information stabilizes 			
NEC, samples 20 ′79	• pin-compatible with EMM Semi Inc's 8108			
(1000 Live in 1000)	SOURCE: ELECTRONICS			

iary of U. S. Philips Corp. intends to be in the ball game. Already shipping 16-K dynamic RAMs, it expects to see working 2147 parts by summer's end, with production volumes by the new year.

Signetics adds MOS to bipolar

Statics seekers get a bipolar choice at Signetics: both TTL and ECL parts. Unfortunately the company has suffered a production setback because it has gone into redesign of its bipolar process. However, production should resume in the coming months. Napoleone Cavlan, marketing manager for bipolar memories, says demand is great enough for versions of the Fairchild 1-K 93415 that Signetics plans to go ahead with its model, the 82S10. He foresees demand in other sizes, so the firm will be making 256-by-8-bit and -by-9-bit parts.

Cavlan expects his firm to forge ahead for a 1980 introduction of a 4-K bipolar part to be competitive with the 2147. The pressure from MOS chips will not come down to speed, but will stay on density, he says. "Still, it's not unlikely that we will have a bipolar 16-K-by-1 part by the end of 1980."

Also in his jurisdiction are the ECL static parts. Offering a 256-bit chip compatible with the 100K family of logic parts, Signetics will bring out a 1-K-by-1 RAM later this year. It will have a maximum access time of 15 ns.

National sees squeeze on TTL

At National Semiconductor Corp., the opinion is that fast ECL and thrifty MOS are squeezing out TTL. As early as August 1977, the firm scrapped plans to build the bipolar 4-K 93415, says Frank J. Barone, director of the bipolar memory division. "We just decided there was no window for it."

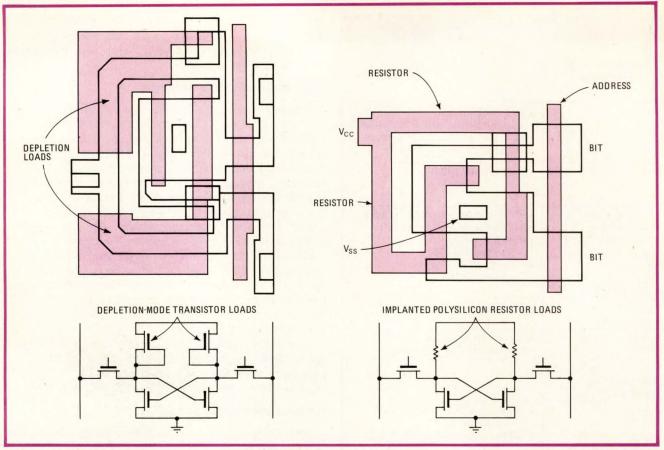
The Santa Clara, Calif., firm's guns are fully trained on ECL. "We're not after very high density—that's for MOS, and treading on MOS is dangerous," Barone says.

The 10422, a 256-by-1-bit ECL part, can be mask-programmed for compatibility with either the 10K or 100K ECL families. Its access time is still a conservative 25 ns. "However, we've only begun to apply the tricks of TTL, like oxide isolation, to ECL," Barone says. "Our goal will be well below 10 ns." As well as boosting speed, these improvements will cut power, reduce die size (and hence price), and make possible the 4-K RAM National expects to bring out in 1980.

The impetus for National's ECL program comes from the changing face of computer technology, says Pierre Lamond, vice president and technical director. "The powerful, mainframe-replacing minicomputers, like those in our own computer group, have revitalized the computer industry in general," he explains. "And they're starting to use ECL."

Another reason for the company's shunning of TTL memories is because it is getting its MOS act together. Moving on from a host of slower statics, including a 2114 with polysilicon loads, it is very close to offering samples of its 2147. Like Motorola, National carried out dual development, settling on depletion loads rather than polysilicon resistors for initial production offerings.

"We're committed to the 2147," says Andrew G. Varadi, director of memory components. "We're looking



4. Watch the loads. The smaller die size of polysilicon load resistors (right) in comparison to depletion-mode transistor loads (left) is an advantage in the design of an MOS static RAM memory cell. Polysilicon expertise will be essential for the next generation of statics: the 16-K.

at various configurations of 16-K parts after that." A year will go by before any part with a spec below 55 ns appears, he adds.

The 2147 will be the first memory to use X-MOS, the name National is giving to its high-performance n-channel process. Starting point is a channel length of about $3\frac{1}{2}\mu m$, but that eventually will be scaled down to $2\mu m$ as the company brings up its DSW equipment.

The future does not hold a version of Intel's 2115 1-K static RAM, even though the bipolar group will not make a version of Fairchild's 93415. Fast RAM plans at National, though, do include larger memories with by-1 and by-4 organizations.

Mostek goes its own way

While Mostek Corp. is pursuing a 2147 part, the Carrollton, Texas, company is also taking a unique route to the high-speed RAM arena. It is promoting a 1-K-by-8 organization for its statics, the 4118 and 4801. The two products are functionally identical, but are cast with different processes and are aimed at different markets.

The 4118 carries access-time ratings that range from 120 to 250 ns, so it is a memory for minicomputers or slower mainframes—or one that is more than adequate for microprocessors. It is built with Mostek's Poly R process, using polysilicon load resistors.

The 4801 will be the first memory to use Scaled Poly 5, which is Mostek's high-performance process that ultimately will be shifted to DSW equipment for scaling of

channel lengths down to 2 μ m. The 4801 will carry 55-, 70-, and 90-ns specs, with samples of the 55-ns version available in a few months.

Both RAMs are fully static parts, relying on what Mostek calls an address-activated system to reduce dissipation when the device is inactive. The parts go into a standby mode, reducing power about two thirds, soon after the signals on the address lines have settled.

The die size of the 4801 is just under 20,000 mil², making it smaller than Intel's 4-K 2147. The polysilicon load resistors help the density, as does the Poly 5 process, which fixes channel lengths at around 3 μ m. Also, Mostek made some changes in the basic static cell circuit (Fig. 3): the load resistors in the flip-flop are connected to a data line, rather than to the positive power-supply line as is the convention. This circuit twist adds significantly to density, since the cell can be smaller if the V_{∞} line does not run through it.

Meanwhile, another group at Mostek is working on a version of the 2147: the 4147, samples of which will be available this summer. Richard Lee, product line manager for statics, explains that his company wants to be in both camps: "Designers of caches and buffer memories have different preferences. Those designing larger arrays will use the 4-K-by-1; but if the depth is less than 4 kilowords, then a 1-K-by-8, like the 4801, or a 2-K-by-8, or even a 4-K-by-8 part is preferred. We want to supply parts for both designs."

As can be inferred, Mostek's plan beyond the 4801

will be a 4802 2-K-by-8 RAM sometime in 1980 and a 4-K-by-8 part after that. Over in the 4147 group, Lee adds, the plans are as straightforward. A 16-K-by-1 part, the 4167, will materialize next year.

Mostek will be looking for finer lines with scaled Poly 5 on both the 4801 and 4147. Eventually, the 4147 will be just larger than 10,000 mil² (that will put the 16-K part in the high-20,000-mil² range) and the 4801 will descend to 14,000 mil².

Semi was early entry

A good deal ahead of the industry, in February 1976, EMM Semi Inc., Phoenix, Ariz., began shipping a sub-100-ns 4-K-by-1 clocked static RAM. Although Semi produces more static RAMs than any other manufacturer and thus has more experience, it has not pushed the speed of its parts.

The problem has been chiefly limited fabrication facilities committed to an extraordinary amount of static RAMs with nonstandard pinouts. Armed now with a new wafer-fabrication plant that will more than double capacity, plus the confidence of a strong, seasoned design team, the well-respected RAM producer will begin to address the high-speed market where most of the MOS action is still talk.

The subsidiary of Electronic Memories and Magnetics Corp. is indeed aiming at the high-speed target, says Fran L. Krch, director of marketing. "Right now, we have the modeling and process work going on to take us down to the 50-ns range." He intimates that the new parts may tend toward the standard-product lineup. "We have [Intel's] 2115 under consideration, and we're also looking at a 2147-type part," he says.

V-MOS still in the groove

V-groove MOS offers higher density than standard n-channel MOS, and those systems designers whom American Microsystems Inc. has convinced of the theoretical advantages are waiting anxiously for proof of the pudding. Well, AMI has spread around enough 1-K 2114Hs to prove they exist; they carry a 70-ns access time and have a memory-cell size of a scant 1.95 mil².

The clincher is that the Santa Clara, Calif., company is among the very few to have provided customers with samples of a 4-K 2147 design. Also using the 1.95-mil² cell, it is a tiny 14,000 mil², as against Intel's 25,000 mil².

The speed distributions on the production line are just starting to throw enough 2147s into the 55-ns bin for volume offering, says T. J. Rodgers, manager of development in the memory division. As well as V-MOS, the polysilicon load resistors contribute to the small size, Rodgers says—AMI and Intel use the same relative lithographic resolution of $4.5 \mu m$.

AMI intends to offer a mixed bag of differing power dissipations and speeds at the 4-K level, as well as a 2147 version with no power-down feature. Meanwhile, it will be perfecting the 1.95-mil² memory cell, then spin it off into all statics, including slower, byte-wide memories for microprocessors and high-speed 1-K and 4-K memories.

A good part of the cell development concentrated on the polysilicon load resistors, which Rodgers maintains must be used in future generations of static memories (Fig. 4). In due course, reduction of geometries from the conservative 4.5 μ m, together with tweaking of the basic cell design, will drive the company's static RAMs down into the 20-to-30-ns territory.

Another trick up AMI's sleeve: the company has developed a 150-ns 2-K-by-8 static, using a double polysilicon process. The part boasts a 1.3-mil² cell, and it should spin off into a next-generation, high-speed 16-K-by-1 static.

If any move could put teeth into the market viability of V-MOS, it will come from Texas Instruments Inc. Admittedly behind in the development of high-speed RAMS, TI has spent the last 18 months playing catch-up ball on two fields: V-MOS and the company's own high-performance n-channel process it calls S-MOS.

Both development tracks have yielded buildable versions of the elusive 2147 that meet the Intel 55-ns spec. However, the Texans find themselves on the horns of a dilemma: they must settle on one design, says Richard Gossen, manager of the MOS memory division in Houston. "We were hoping that one of the approaches would show a clear margin above the other, but the economic data have been too close," he says. "It's hard to weigh the smaller size of V-MOS against its epitaxy and anistropic etch—a more complicated process than with S-MOS."

TI faces a decision

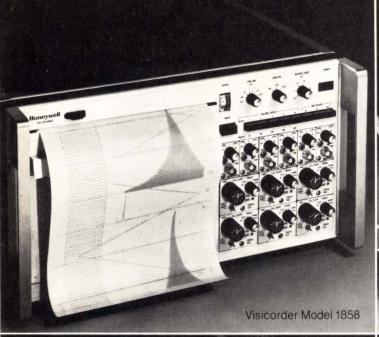
TI can support only one such long-term commitment to its customers, according to Gossen. That decision will come in the next few months, and it is not to be taken lightly. The process technology chosen will eventually be the mold from which TI will cast all its static RAMs.

Like others, the Dallas firm is looking for very high performance from MOS devices. "But we can't wait to get there by going through the continuum of development," Gossen maintains. "We'll build the 2147, of course, because it's in high demand. But really it's just the means to an end for us. We have to make a very deliberate shot at the 20-to-30-ns market." Like others, he sees a clearly segmented static RAM business: below 55 ns and then up at the slower end of the range where TI has been supplying 150-ns 4-K parts for some time.

Of course, the high-speed end is requiring a huge effort, but development in the two speed extremes is not entirely unrelated. As have other manufacturers, TI used the slow end as a training ground. Its 150-ns 2-K-by-8 TMS 4016 static memory [Electronics, July 20, 1978, p. 39] was a combined salvo aimed at boosting density and lowering cost.

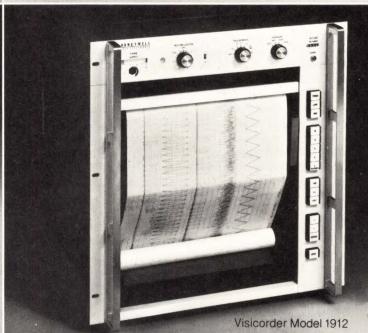
This extremely ambitious part only recently began showing respectable yields, but its 1.6-mil² cell size strongly undercuts that of the 4.3-mil² 4-K TMS 4045. Yet the new part uses the same 4.5-\(mu\) m line widths as the 4045 which is TI's version of Intel's 2114. The small cell size, the result of a redesign that folded the load resistor back onto the transistors, will be fanned out through existing moderate-speed parts and is the seed for TI's sub-50-ns efforts.

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C-MOS codec solves phone line problems with bipolar interface

Three-chip low-power channel unit handles high-voltage transients

by Steve Kelley

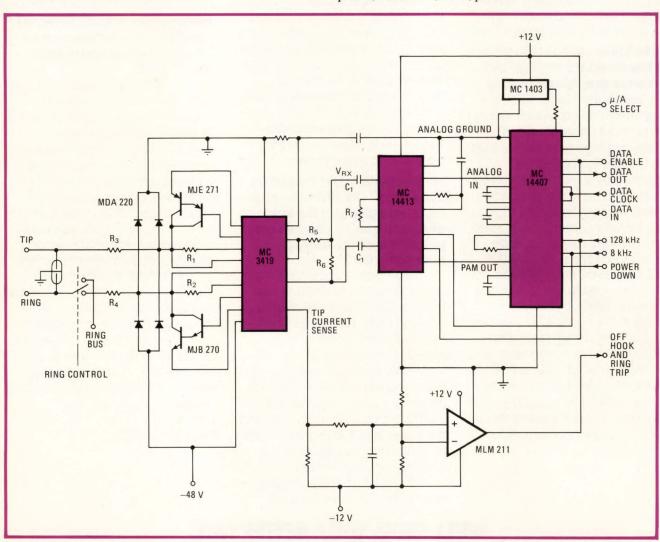
Motorola Inc., Semiconductor Group, Phoenix, Ariz.

☐ The typical codec does not slip unaided into existing telephone networks, being unable by itself to provide the benefits of full-duplex voice digitization in a time-division multiplexed switching system. The lonely codec needs some help with two major circuit functions that must be handled in the standard telephone interface. Frequency-limiting filters are needed to allow the codec to sample the analog voice signal without spurious response generation. In addition, a two-to-four-wire converter and line feed circuit are needed in order to eliminate a bulky transformer connection in the line leading to the telephone.

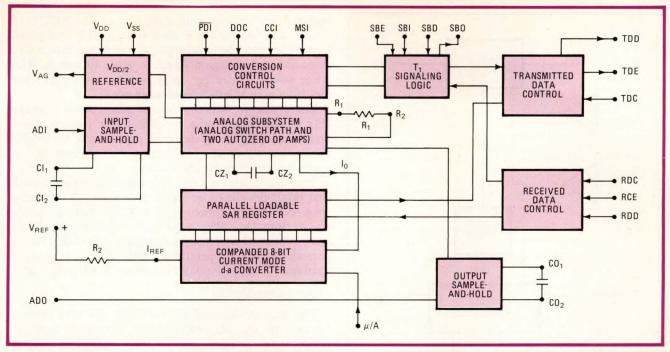
Unified approach

If digital telephone equipment is to take its place in the industry, it is necessary to address the problem of the complete subscriber channel unit needed in a modern digital switching office. Motorola Inc.'s Semiconductor

This is the sixth part of a series on the new integrated-circuit codecs. The other articles have appeared in the issues of Sept. 14, 1978, p. 108 and 111, Sept. 28, p. 141, Oct. 12, p. 130, and Feb. 1, 1979, p. 126.



1. Subscriber channel unit. Up to 1,900 ohms of resistance can accumulate in the wire pair leading from the tip and ring connections in an individual subscriber telephone to the codec circuitry in the local telephone office. This long connection is a chief source of telephone troubles.



2. What's inside. The various companding functions of the MC14406/7 codecs are implemented with metal-gate C-MOS because they are most reliable and easy to design in this technology. The analog voltage V_{AG} provides a ground reference signal for the other two chips.

Group has developed a three-chip approach to complete channel unit design, using a combination of bipolar and complementary-metal-oxide-semiconductor technology.

The MC14407 codec is a single-chip full-duplex C-MOS device that offers pin-selectable A- or μ -law companding in a 24-pin package. The MC14406— μ -law only—has additional signaling capability required by μ -law specifications and needs a 28-pin package. Each codec operates from a single supply voltage with an on-chip voltage regulator for analog ground. Normal operating power is less than 90 milliwatts; the codecs use less than 1 mW in the standby mode. The other members of Motorola's codec trio are the C-MOS MC14413 switched-capacitor filter and the bipolar MC3419 subscriber loop interface circuit (SLIC).

The C-MOS process was chosen for the companding chip because all the necessary digital-to-analog converters, operational amplifiers, voltage regulators, and comparators are available in this technology, satisfying the codec's need for precision analog circuitry. The complementary nature of C-MOS switches, amplifiers, and logic allows the low-power operation that is necessary for efficient use of many codecs in large telephone switching systems.

C-MOS reliability

Motorola's metal-gate C-MOS process has been in production for more than eight years. It has a proven history of high reliability behind it and readily meets the stringent reliability requirements of the telecommunications industry.

In the usual telephone subscriber hookup (Fig. 1), the standard L_1 and L_2 telephone terminals are connected through wire with up to 1,900 ohms resistance to the tip and ring terminals of the subscriber channel unit. Two-way voice transmission, signaling, and power are all

supplied to the subscriber's telephone through this single pair of wires.

At the digital end of the channel unit, the codec is connected to a high-speed digital highway with separate data buses for transmitting and receiving. An enable signal from the switch controller tells the codec to transmit a serial 8-bit word on the transmit bus and to receive one from the receive bus. These 8-bit words are coded representations of the voice signals on the two-wire pair.

Digital control

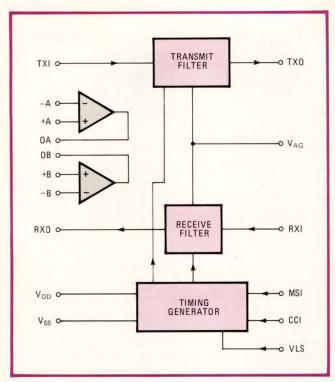
There is also a low-speed digital highway between the channel unit and the office control system for supervisory and control signals. Dialing pulses, ringing control, requests for service, and various test modes all appear as binary numbers on the digital office side of the channel unit circuitry.

In the codec itself (Fig. 2), the transmitted-data and received-data control lines (TDE and RCE) handle the digital input/output interface. They use independent data clocks—one for transmitting, the other for receiving—that run at rates up to 3 MHz. The rest of the circuit is controlled by a 128-kHz conversion clock (CCI).

An analog subsystem provides autozeroing and signal-path control to and from the 8-bit companding digital-to-analog converter. An 8-bit parallel-loadable successive-approximation register manipulates data in the d-a converter for both transmitting and receiving functions. Additional logic is provided for signaling data, power-down, and other telephone functions.

The compandor's d-a converter is built with stacked 8-bit and 6-bit matched-device arrays. This structure provides direct, inherently monotonic companding. The d-a converter is fully static and its output is a precision current similar to that of bipolar d-a units.

The advantage of this current-steering d-a converter is



3. No spurious responses. The two antialiasing filters employs switched-capacitor technology, which offers more attractive characteristics than the charge-coupled-device approach. Each chip has two extra operational amplifiers that are used in the channel unit.

that it may be statically tested with 8-bit words applied through the data-receiving logic of the codec. The current output of the d-a converter is available at the codec's R_2 pin. Its static accuracy is testable after product assembly; in fact, an external current-to-voltage converter at R_2 bypasses the zeroing circuitry, allowing a fully static test. Capacitive-array d-a converters must be tested dynamically—no existing resistor-string approach allows static testing external to the packaged part.

Considerable margin over the performance requirements is achieved in the μ -law device's measured signal-to-noise ratio performance. The A-law characteristic yields similar results. Idle-channel noise with zero input signal is typically 0 dBrn for both μ and A laws, thanks to the autozeroing method chosen. Gain tracking performance for both μ - and A-law devices is also well within specifications.

Independent analog ground

The codec uses its on-chip voltage regulator to produce a $(V_{DD}-V_{SS})/2$ analog ground output. All of the analog circuitry operates with reference to this internally generated supply; external filters and hybrids may use this output as a ground reference. The on-chip regulator allows the codec to operate from a single 10- to 16-volt supply. A channel unit consisting of codec, filter, SLIC, and reference voltage can be assembled using the codec's V_{AG} output as the channel unit's own independent analog ground. This avoids ground loop connections among the system's channel units that might cause crosstalk.

The rationale behind the use of C-MOS technology for the codec compandor is even more convincing for the required antialiasing solid-state filters. The MC14413 C-MOS switched-capacitor filter is an analog integrated circuit that uses the advantages of complementary active loads in the C-MOS gain stages to great advantage. The lower power needed per stage results in a design that dissipates only 30 mW overall when active.

The transmit filter section of the 16-pin package (Fig. 3) is composed of a five-pole elliptic low-pass filter and a three-pole Chebyshev high-pass section. It samples the applied signal at 128 kHz and thus requires only a

single-pole prefilter for antialiasing.

The receive filter is a five-pole elliptic low-pass section that resamples the codec signal; it includes all necessary frequency compensation. The 128-kHz full-duty-cycle signal from this filter requires no postfiltering to be compatible with system specifications. The design incorporates 16 C-MOS operational amplifiers, two of them uncommitted units available for interface with the SLIC.

Filter compatibility

The filter is designed to be compatible with various features on the MC14407 codec. Operating synchronously with the codec, proper filter operation requires both the 8-kHz sync and 128-kHz conversion clock. It can operate with a dual supply of ± 5 to ± 8 V, but uses the V_{AG} output of the codec as a ground so that only the single codec supply of 10 to 16 V is needed. A codec power-down also brings the filter down to a 1 mW consumption level through the V_{AG} input.

The filter's switched-capacitor techniques offer certain inherent advantages for codecs in pulse-code modulation systems. They allow high sampling rates without the antialiasing front ends required in charge-coupled-device designs. Furthermore, the phase response of a switched-capacitor filter is naturally near the desired minimum phase design: the large group delay of linear-phase CCDs need not be overcome.

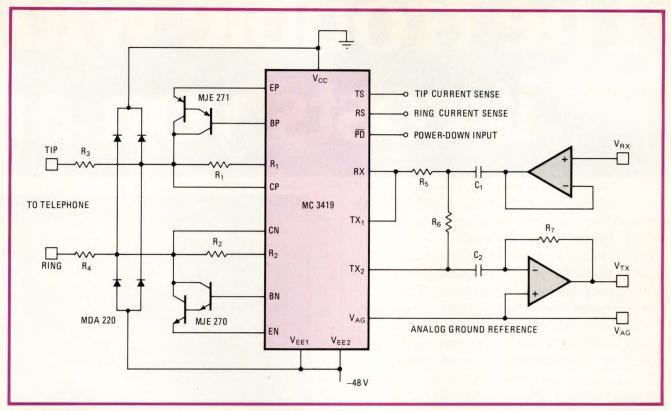
Subscriber line interface

The subscriber channel unit must ultimately interface the standard telephone wire pair. Unfortunately, the equipment environment changes drastically on the telephone side of the filter. Telephone pairs with a typical 1,900-ohm resistance depend on a 48-v battery to inject sufficient current into the telephone to make it function.

The 18-pin MC3419 and its associated circuitry are designed to operate from that 48-v battery and to withstand lightning and faults, as specified for the outside-plant interface. These voltage and transient requirements mean that bipolar technology must be used instead of C-MOS.

Decoded and filtered signals from the digital highway arrive at the receiving terminal (RX) of the SLIC as an analog voltage (Fig. 4). The RX pin has a low impedance, so the signal current injected into the SLIC is determined by R₅.

Two power transistors drive the parallel combination of loop and SLIC termination with signal current. The current flowing in the SLIC termination causes signal current at TX₂ which is out of phase with the current at RX. Resistor R₆ is selected to cancel that signal to achieve transhybrid rejection. Signals from the telephone



4. Two becomes four. The subscriber line interface circuit provides the impedance conversion from the two-wire hookup in the individual telephone to the four-wire system in the codec and telephone office. It is made with bipolar technology because it has to handle 48 volts.

cause current in R_1 and R_2 and consequently signal current at the TX_2 pin.

This uncanceled component is converted to a voltage in R₇, providing the signal to be transmitted via the filter and codec. The two uncommitted op amps on the MC14413 can be used as the op amps shown in Fig. 4. Selection of R₅, R₆, and R₇ adjusts the channel unit's gain for both transmitting and receiving.

On the two-wire side of the SLIC, both the feed resistance and termination resistance must be synthesized with R₁ through R₄. For a 400-ohm feed and 900-ohm terminations, for example, R₃ and R₄ are set at 30 ohms and R₁ and R₂ at 16.4 kilohms. A short loop connection will draw 120 milliamperes from the battery with 118 mA supplied through the MJE270/271 transistor pair. Only 2 mA will flow in R₁ and R₂, so they can be quarter-watt devices. In the short-circuit state, the transistors dissipate 2.5 watts each while the MC3419 uses only 0.5 W. The SLIC thus has resistive feed and can be designed for any feed resistance value by proper selection of resistors R₁ through R₄.

The MDA 220 diode bridge and feed resistors R₃ and R₄ provide various forms of hazard protection for the channel unit. The diodes are rated to take the 50-ampere surges of 1,500-v lightning transients. Intermittent power line contact will generate similar surges and 4 A of continuous current; this is also within the diodes' rating. Extended power line contact will destroy the resistors without damaging the diode bridge or other portions of the channel unit. In the normal operating mode the diodes are back-biased and the resistors contribute the feed and termination impedances for the SLIC.

Another common external hazard is a short circuit to ground of either the tip or ring lead. When the MC3419 SLIC is used, a ring or tip lead faulted to ground in any combination will draw only 10 ma. The worst-case unprotected fault condition is a short circuit between the ring and tip lines, which draws only 120 ma.

Requests for service, dialing pulses, and ring trip signals can all be handled by the SLIC's loop sensing outputs. The TS and RS leads provide switch hook status information to the central office. Only a 20-Hz, 120-v rms ringing signal must be provided externally. A single-pole double-throw relay in series with the ring lead is required to accomplish this.

Putting it together

A complete telephone-to-digital-highway channel unit with unique features is possible using the MC14407, MC14413 and MC3419 trio as a package. The MC3419 circuit uses no power with the phone on the hook; the codec and filter may also be powered down with a logical input when they are not in use. If the codec and filter are powered up while the phone is on the hook, a unity-gain loop-back is created at the SLIC interface. This allows for automatic diagnostic testing by the operating telephone company.

An idle channel unit will consume less than 10 mW when powered down. The design of an economical digital telephone office is not dominated by codec selection alone: the cost of the entire subscriber channel unit's function must be considered. This can be easily done with this three-chip set's unified approach to the telephone-to-digital-highway interface.

"The trouble with it costs you an

A natural assumption. Name anything that's tailor-made for you, and you expect it to cost more than the off-the-shelf model.

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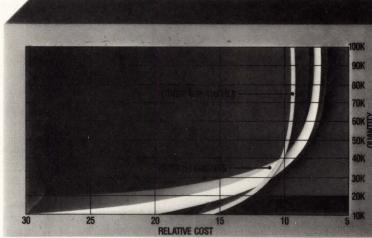
So, to get right down to the bottom line, you have to weigh all the hidden expenses. Not simply the number of parts involved. But also board space, assembly time and testing, which can run you as much as 50% of the cost of the circuits themselves. Then throw in warranty, service, spares and, for microprocessor systems, software development, and you may well discover that custom turns out to be the most cost-effective way to go.

"How do I know what's best?"

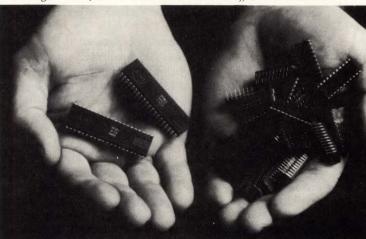
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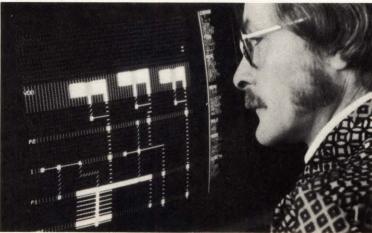
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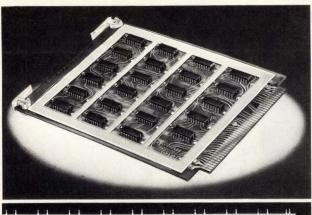
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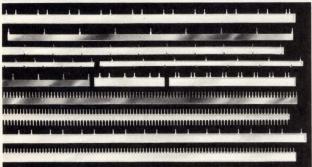
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LSI streamlines instrument interface with standard IEEE-488 bus

Highly flexible design enables large-scale integrated circuit to link most microprocessor-based instruments to popular bus

by John Pieper, NV Philips Gloeilampenfabrieken, Almelo, the Netherlands and Robert J. Grossi, Philips Test & Measuring Instruments Inc., Mahwah, N. J.

□ With the acceptance of the IEEE-488 bus for automatic measurement systems, the demand for instruments incorporating this standard is almost universal. However, the growing use of microprocessors in recent instruments makes implementation of the interfacing tricky. In particular, matching an instrument's internal buses to the external IEEE-488 bus is difficult when the buses differ in the number of their lines and operating speed.

Until recently, instruments capable of this interface needed as many as 45 additional transistor-transistor-logic circuits, making the overall design very complex and expensive. Philips has therefore developed a single large-scale integrated circuit that provides all the required coding, decoding, and interface functions. The designer is thus free to concentrate on the performance of the instrument itself.

The chip, designated the HEF 4738, comes in a 40-pin dual in-line package. It is made using Philips' LOCMOS (for local-oxidation complementary-metal-oxide-semi-conductor) technology, which is as fast as transistor-transistor logic but with lower power consumption, as well as higher circuit density.

The HEF 4738 gives the designer a great deal of flexibility, since it can both drive and be driven by C-MOS, TTL, or low-power TTL devices. It operates from

supply voltages between 4.5 and 15 volts. The outputs to the bus drivers can drive one standard TTL load; all others can drive two low-power Schottky TTL loads. Quiescent power dissipation for the entire package is 1 milliwatt; typical dissipation is 30 to 50 mw. Transmission rate of the DIO lines is 200 kilobytes per second.

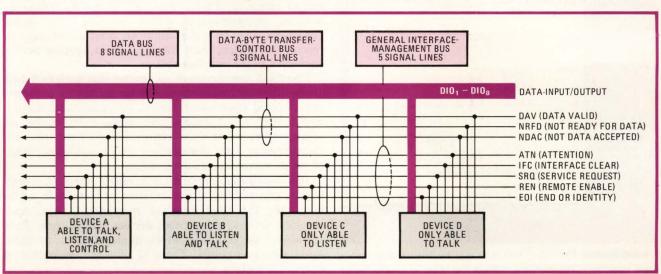
The device may be operated in ambient temperatures of between -40° and +85°C. It comes in a plastic or a metal-ceramic package [Electronics, Feb. 15, p.181].

To design an instrument for compatibility with the IEEE-488 bus, be it counter, multimeter, or waveform generator, a clear understanding of how the bus operates and how the HEF 4738 can implement the required interfacing is needed.

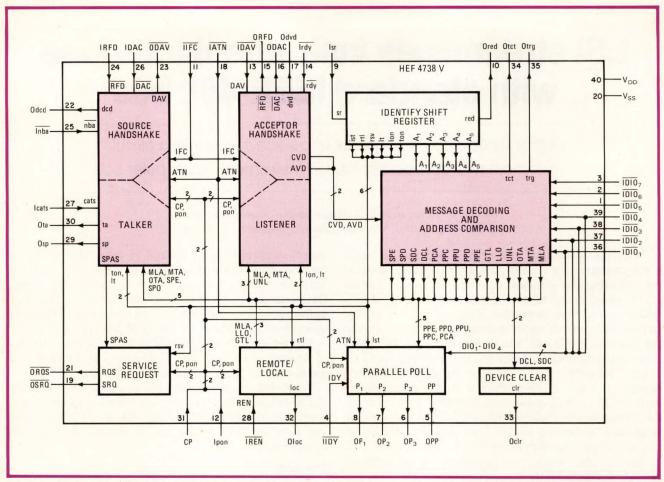
The bus

Figure 1 shows the basic structure of the IEEE-488 interface bus system. Its 16 lines permit a maximum system configuration of 15 devices. The bus lines break down into three sections, consisting of eight data lines; three data-byte transfer control lines, also known as the handshake bus; and five lines for general interface management, designated the management bus.

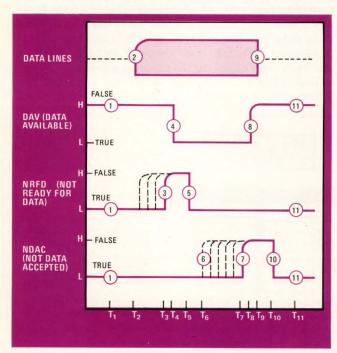
Four types of device can be connected to the bus. Those which only transmit bus data (done upon demand)



1. Bus basics. The 16 lines of the IEEE-488 interface bus are divided into three segments to control up to 15 devices. The four basic device categories are represented at the bottom of the diagram. Each bus line is named after the function performed by the signal it carries.



2. Internal layout. The HEF 4738 bus interface chip is organized in 10 functional blocks. The bus signals (all capital letters) applied to the chip are inverted by inverting transceivers, not shown. Signals are prefixed with I or O to designate input or output signal flow, respectively.



3. Handshaking. The four signals represent the listener-talker handshake operation. The numbers indicate the order of events taking place. For more than one listener, the waveforms for the NRFD and NDAC signals are composite because of the different response rates.

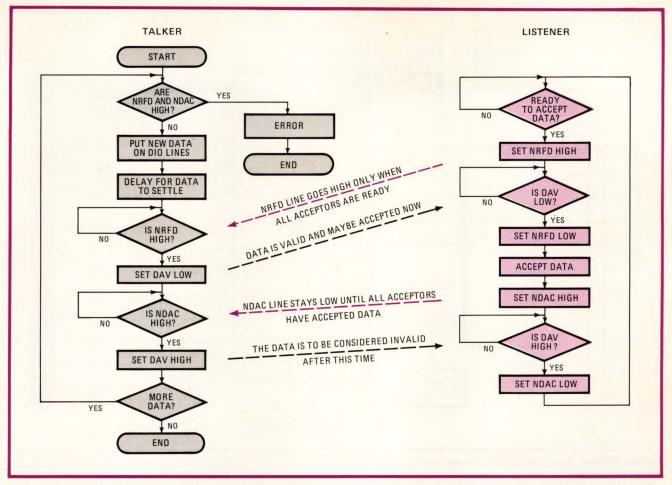
are called "talker" devices. Such a device—for example, a nonprogrammable digital voltmeter or frequency counter—can be addressed by an interface message to send device-dependent messages to another device connected to the bus.

Devices that only receive data on the bus make up the second category. These "listener" units—for example, printers, programmable power supplies, and signal generators—can be addressed by an interface message to receive device-dependent messages from another device connected to the interface system.

The third group consists of devices that both talk and listen, allowing measurements to be made and parameters changed upon command. A programmable digital multimeter, for example, can change its range or measurement mode upon command and then transmit measurement data representing either millivolts, megohms, or microamperes upon request.

The fourth type performs the control function. These devices can address others to listen or to talk. In addition, they can send interface messages to command specified actions within other devices. These controllers are usually desktop calculators, minicomputers, or dedicated microcomputers. There is only one controller in charge per system.

The IEEE-488 interface bus defines eight data lines that carry information asynchronously in a bit-parallel,



4. Bus conversations. The flow chart describes the sequence of events between a listener and a talker during the handshake operation. The data-valid, not-ready-for-data and not-data-accepted lines of the data-byte transfer-control bus ensure information-transfer integrity.

byte-serial form in both directions. The data bus lines are used for carrying all interface and device-dependent messages.

Figure 2 is a functional block diagram of the HEF 4738. Note that the chip's interface signals are positive logic, whereas the 488 bus signals all are negative logic. The signals in the chip must therefore be inverted by inverting transceivers (not shown here). They are prefixed by I or O, designating input or output signal flows, respectively. Capital letters indicate chip-to-bus (external) signals, and lowercase letters represent chip-to-device (internal) signals.

Only seven data lines are needed for all messages to the interface. The data-input/output bus lines (DIO_1-DIO_7) connect to the chip's respective inverted-data inputs ($\overline{IDI}_1-\overline{IDI}_7$) at the locations shown,

Controlling the data flow between devices is a handshake process operating over the three lines of the databyte transfer-control bus. These lines effect the transfer of each byte of data on the data lines from a controller or a talker to one or more listeners.

Each of the handshake bus's three lines is named for the signal it carries. The data-valid (DAV) line indicates the availability or validity of the information on the data bus lines. The not-ready-for-data (NRFD) line indicates the readiness of the device or devices to accept data. The remaining line signals that one or more devices has not accepted data and is called the not-data-accepted (NDAC) line.

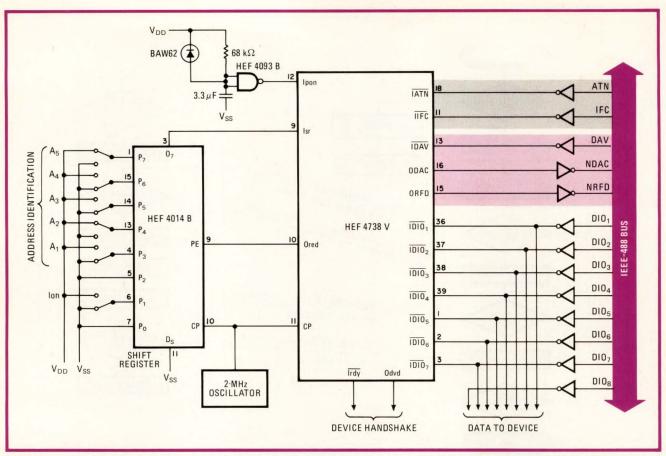
Figure 3 shows the timing diagram of the handshake operation. Based on an interlocking relationship between source (talker) and one or more acceptor (listener) devices, it ensures that information is put on the data lines properly and then removed correctly for decoding.

The source starts the process by setting the DAV line false, denoting the absence of any valid data. Simultaneously, the acceptor that is addressed sets the NRFD and NDAC lines true, indicating that the acceptors are not ready and will not accept any data.

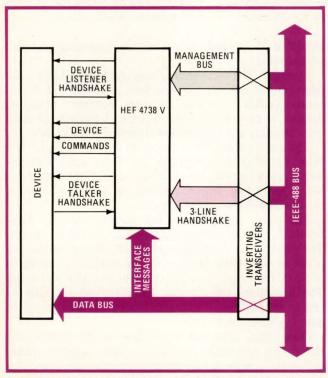
The source then places a new data byte on the data-I/O lines, allowing it to settle for at least 2 microseconds. The NRFD line goes false when all the acceptors are ready to accept the data byte. This causes the source to put DAV true, signaling that the data is settled and valid. The acceptors indicate that they are taking data by setting NRFD true, which also blocks the acceptance of data from another source.

Once all the acceptors have taken the information, the NDAC line goes false. The source then sets DAV false, telling the acceptors that the data is no longer valid. The data may then be changed and the process restarted. The flow charts in Fig. 4 show the sequence of events for handshake process between a talker and a listener.

To accomplish talker and listener interfacing, the



5. Basic listener. The diagram shows the interface for a basic listener device with the IEEE-488 bus using the HEF 4738 interface chip, the HEF 4014B shift register, and the necessary inverting transceivers. The shift register handles the device's internal addressing.



6. Double shake. The block diagram illustrates the HEF 4738's role in interfacing the device with the 488 bus. Two handshake operations take place: one between the measurement device and the interface chip, the other between the chip and the external bus.

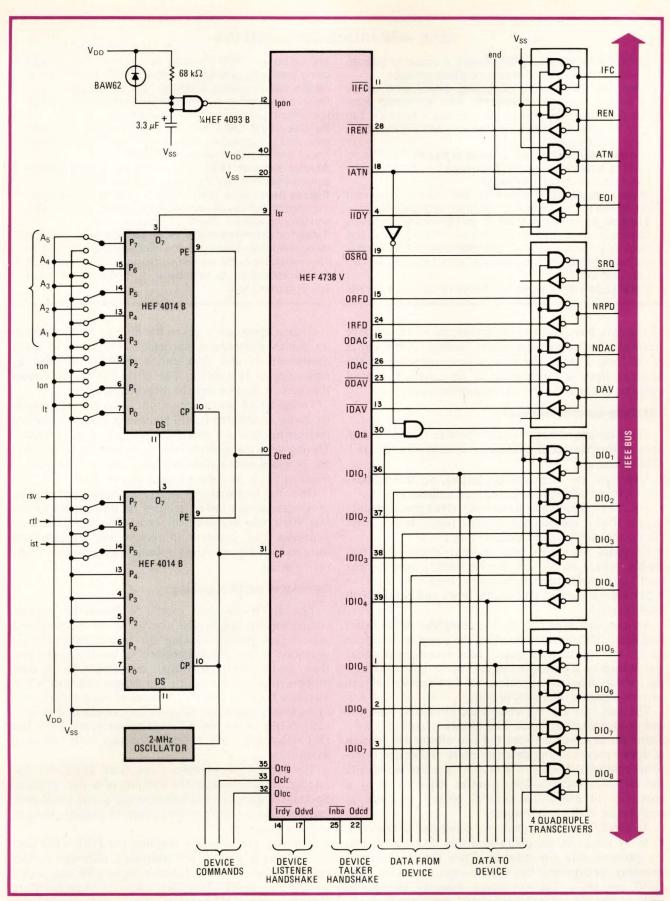
handshake bus's signals are each split into input and output subsets. These subsets interface a source device with an acceptor device over the 488 bus. The source subset comprises IRFD, IDAC, and \overline{ODAV} signals; ORFD, ODAC, and \overline{IDAV} signals make up the acceptor subset. Figure 5 shows the configuration for devices able only to listen using the HEF 4738 and a HEF 4014B shift register.

Another handshake process occurs between the device and the interface chip, as shown in Fig. 6. However, if the device is able to send or receive data within one clock period, these device handshake control signals are not needed and each I/O set can simply be shorted together for the interface to work properly.

If not, the handshaking for the talker setup uses the don't-change-data output (Odcd) signal and the new-byte-available input (Inba) signal. With these signals, the device may change the data only when Odcd is low and set Inba low to indicate that new data is available. The Odcd line can go low only when Inba is high.

The corresponding listener device handshake signals use the data-to-device-valid output (Odvd) signal and the ready-for-next-byte (Irdy) signal to indicate device readiness.

The management bus is a set of five lines used to manage an orderly flow of information across the interface. As with the other lines, the management lines are named for their tasks. The attention (ATN) line is managed only by a controller, to specify if information



7. Talker-listener. Shown is the circuit diagram for a basic talker and listener interface realized with the HEF 4738 interface chip, two HEF 4014 B shift registers, and four quadruple inverting transceivers. The transceivers make the positive (chip) to negative (bus) logic transitions.

IEEE-488 interface functions

Acceptor handshake (AH) enables a device to guarantee correct reception of remote multiline messages.

Controller (C) lets the controlling device send device addresses, universal commands, and addressed commands to other devices over the interface. A controller can only exercise its capabilities when it is sending the attention (ATN) message.

Device clear (DC) allows a device to be reset to an initial state by a remote message. The device may be addressed individually or as part of a group.

Device trigger (DT) allows the controller to command the device to start its basic or programmed operation.

Listener or extend listener (L or LE) enables a device to receive device-dependent data over the interface. This capability exists only when the listen interface function is addressed to listen by a controller or by the local listener-only (Ion) input.

Parallel poll (PP) allows the device to present a parallel

poll response (PPR) message to the controller without being previously addressed to talk. Before performing a parallel poll sequence, a device must be assigned (enabled) to respond on a particular data-input/output (DIO) line either locally or by a remote message.

Remote/local (RL) lets the device select between programing information from device front-panel controls (local) and from the interface (remote).

Service request (SR) lets the device request service actions from the controller (for example, polling).

Source handshake (SH) enables a device to guarantee the correct transfer of multiline messages to one or more acceptor handshake interface functions.

Talker or extended talker (T or TE) lets a device send device-dependent data over the interface to other devices. This capability exists only when the talker interface function is addressed to talk by a controller or the local talk-only (ton) input.

on the data bus lines is to be interpreted as an interface message or as a device-dependent message. If this line is in the logic 1 state, the information appearing on the data-I/O lines is interpreted as an interface control message; if it is in the 0 state, the information is data.

Interface-control messages

The interface-control messages provide remote control through four classes of messages available with the HEF 4738. These are:

- Addresses: my listen address (MLA), my talk address (MTA), other talk address (OTA), and unlisten (UNL).
- Addressed commands: go to local (GTL) group execute trigger (GET), selected device clear (SDC), take control (TCT), and parallel poll configure (PPC).
- Universal commands: local lockout (LLO), serial poll enable (SPE), serial poll disable (SPL), device clear (DCL), and parallel poll unconfigure (PPL).
- Secondary: parallel poll enable (PPE) and parallel poll disable (PPD).

Another line used only by the controller is the interface-clear (IFC) line, for resetting the complete interface system into its quiescent state. The service-request (SRQ) line is used by a device to indicate to the controller that the device requires attention, an interruption of the current sequence of events, or both.

The last two are the remote-enable (REN) and the end-or-identify (EOI) lines. The former is used only by a controller to select between the two alternative sources of device programming data (interface and device front-panel controls). The latter is used by a talker to indicate the end of a multiple-byte transfer sequence or by a controller to execute a parallel polling sequence in conjunction with an ATN signal.

As noted, these five signals are connected to the HEF 4738 by means of the chip's inverting transceivers and are prefixed with I/O notation. Thus the chip's corresponding management bus signals appear as IATN, IIFC, OSRQ, and IREN. The EOI signal, however, changes to IIDY, or identify, since the end signal originates from the device itself after it completes the last task.

System operation is generally initiated by the controller, which programs a particular instrument to make measurements and then passes them to the bus by addressing it as a talker. The controller also addresses the listeners that receive the measurements.

To inhibit all instruments from listening, the controller issues an unlisten (UNL) command on the bus before addressing one or more instruments and listeners. Having sent the address, the controller then transmits the program information in a sequence of data bytes—for example, to perform a measurement.

Once the measurement starts, the instrument may be programmed as a talker, sending its information on the bus when the measurement ends. The controller also addresses new listeners to receive the measurement information. Figure shows a basic listener-talker interfacing setup.

Serial and parallel polling

Ten IEEE-488 bus interface functions provide comprehensive and flexible control of the measurement system (see panel). Linking the instrument's internal operation to the external protocol of the IEEE-488 bus, they enable each individual instrument to receive, process, and send messages. The designer chooses which interface function subsets are required for the particular instrument's operation, since an instrument that is basically only a talker has different requirements from one that is basically only a listener or that both talks and listens.

The HEF 4738 provides these basic IEEE-488 bus interface functions with the addition of a shift register. Special features like local programming and serial polling can also be implemented. Parallel polling, though, requires a decoder.

The only 488 interface function the HEF 4738 does not provide is that of the controller, although it does provide three controller function signals for use with a controller: input-controller-active-or-transfer-state (ICATS), output-talker-active (Ota), and output-take-control (Otct).



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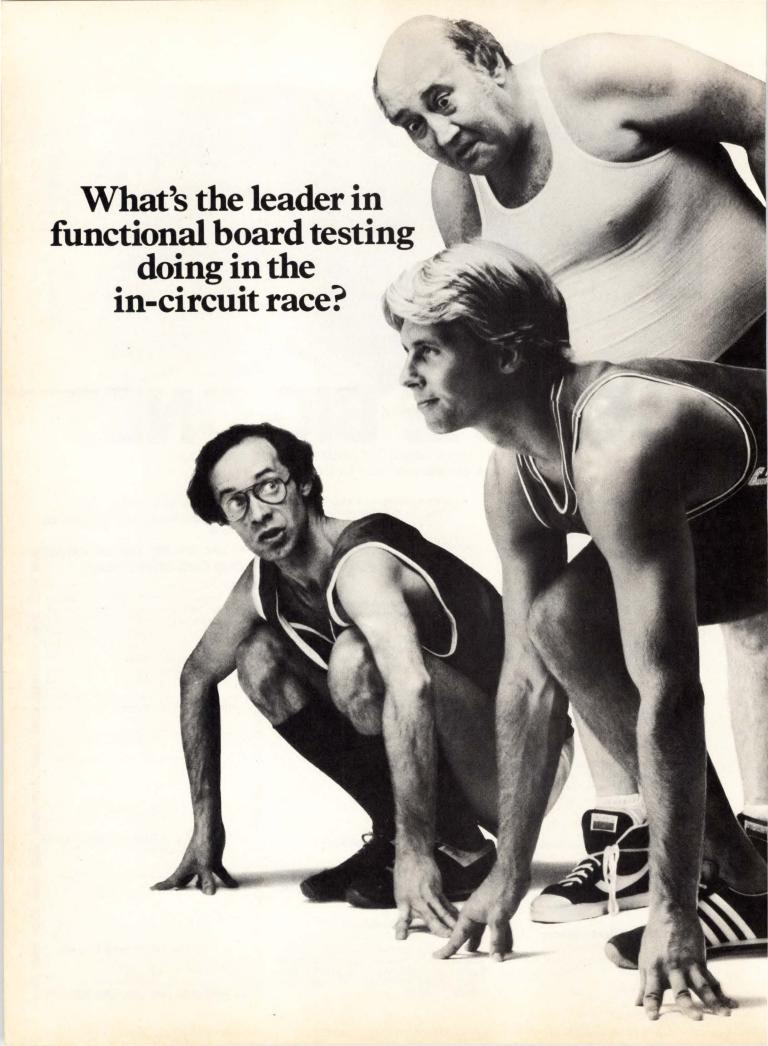
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Engineer's notebook

Dynamic go/no-go checker gauges pulse-width range

by R. E. S. Abdel-Aal Sunderland Polytechnic, Sunderland, England

Because it can determine if the width of a pulse falls between two specified limits, this circuit is useful in tasks like testing the dynamic performance of circuit cards. Using three integrated circuits—one dual monostable, one dual flip-flop, and a quad NAND gate—the circuit can be built for \$5. Three light-emitting diodes indicate instantly whether the pulse width is less than, within, or greater than the specified width, making the circuit ideal for the production line.

The positive edge of the pulse to be measured triggers one-shots A_1 and A_2 , whose resistor-capacitor time constants are set to provide a pulse equal to τ_{\min} and τ_{\max} , respectively. The input pulse, having width τ , is also

applied to the data (D) input of flip-flop A₃.

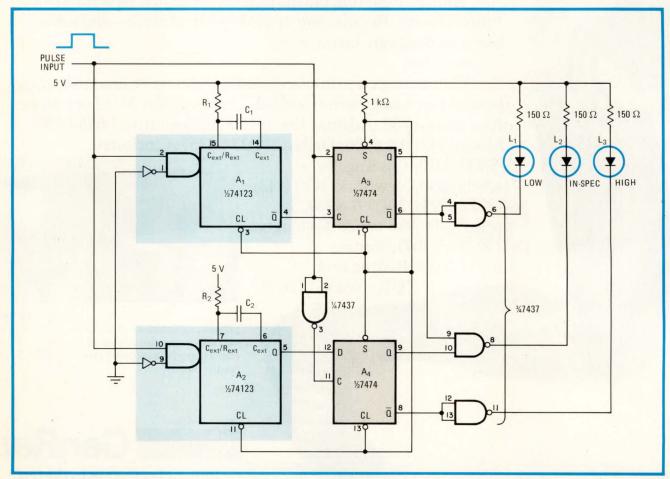
 A_3 's clock input is driven by the \overline{Q} output of A_1 . Thus if $\tau < \tau_{\min}$, there will be a logic 0 at the D input of A_3 at the time the rising edge of the \overline{Q} output of A_1 clocks A_3 . LED L_1 will then light, indicating the input pulse width is below the minimum value set, τ_{\min} .

Similarly, the D input of flip-flop A_4 is driven by the Q output of one-shot A_2 , while the inverted pulse input serves to clock A_4 's C input. If $\tau > \tau_{max}$, LED L_3 will light, indicating the input pulse width is greater than the maximum value set, τ_{max} .

If τ lies between τ_{min} and τ_{max} , the Q outputs of both A_3 and A_4 will move high, activating the NAND gate connected to LED L_2 . This LED will then light. Note that it is not possible for more than one LED to be on at any given instant.

The circuit is self-resetting and can accept the next input pulse to be measured as soon as the one-shots time out.

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay \$50 for each item published.

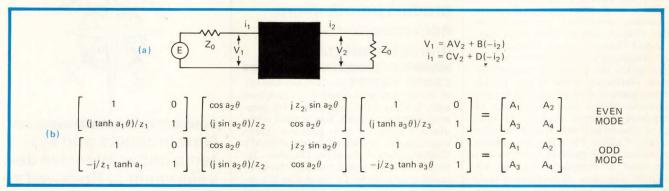


Within limits. Circuit checks if width of test pulse is less than, within, or greater than two specified values, τ_{\min} and τ_{\max} . RC elements of one-shot A₁ set τ_{\min} ; corresponding components of A₂ set τ_{\max} . Three LED's provide instant and direct indication of pulse width range.

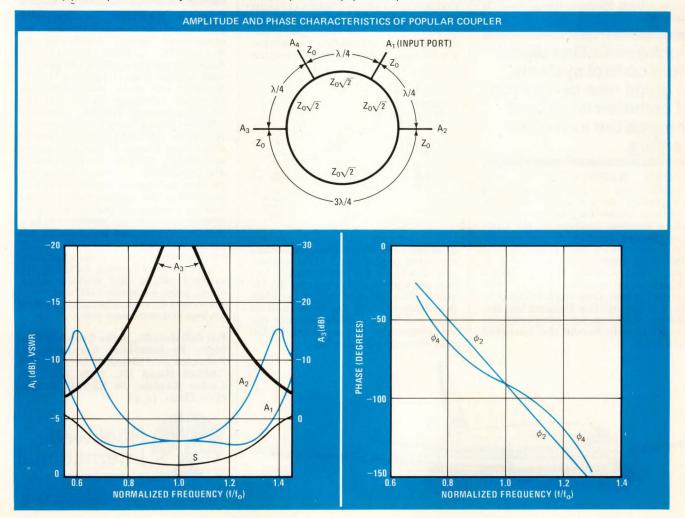
HP-97 finds response of microwave couplers

by J. Saillard, Université de Rennes Rennes-Cedex, France Finding the amplitude and phase of microwave energy at the output ports of rat-race and other symmetrical couplers is fast with this program. Given the coupler's matrix elements, the program generates the required data for any normalized frequency. It has been designed to accommodate the entry of a series of frequencies so that curves for the coupler can be plotted.

A four-port network is defined by the two equations



Matrix manipulation. Equation set for general four-port network (a) is converted to equivalent matrix equation for considering circuit behavior at high frequencies, where all matrix parameters are defined in text. When a symmetrical coupler is considered, matrix expression becomes (b), the equation solved by the HP-97. Plotted response of a popular coupler is shown in illustration below.



GROWTH SPURS HIRING

Rockwell Plans For Continued Avionics Growth In 1979.

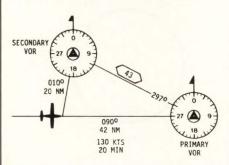
CEDAR RAPIDS - Rockwell International is anticipating another year of growth and new developments for its avionics and telecommunications businesses, according to sources in Cedar Rapids where Rockwell's Avionics and Missiles Group is headquartered. Rockwell's Collins Divisions have helped place the company among the largest electronic firms in the world. The company is now gearing up for development of the next generation of electronics products. Among the systems produced in Cedar Rapids are the Rockwell-Collins Pro Line and Micro Line avionics for general aviation air-craft, and a complete line of air transport avionics. Government avionics products and systems include the U.S. Air Force standard tactical air navigation system, and the complete avionics system for the new U.S. Coast Guard Medium Range Search Aircraft.

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from two VOR stations to compute distance and groundspeed. (The engineer who developed the latter product was named Engineer of the Year for the Division.) The thrust of the new product development work for both product lines will be to further increase the momentum that has propelled the Division to market leadership.





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010	008	STO7	046	→P	084	RCL1	122	2	160	1	198	RCL5
011 ENT↑ 049 STO3 087 TAN 125 STO0 163 RCL9 201 RCL4 012 COS 050 X ≠ Y 088 ÷ 126 X ≠ Y 164 — 202 — 013 STOE 051 1/X 089 + 127 STO1 165 ÷ 203 → P 014 X ≠ Y 052 STO2 090 GSBB 128 RCL3 166 PRTX 204 X ≠ Y 015 SIN 053 RCLB 091 P ≠ S 129 RCL2 167 RCL3 205 PRTX 016 RCL4 054 RCLC 092 RCLB 130 → R 168 RCL7 206 X ≠ Y 017 X 055 — 093 RCLC 131 STO2 169 + 207 LOG 018 STOB 056 RCLA 094 + 132 X ≠ Y 170 RCL2 208 2 019 RCL6 057 RCLD 095 RCLA 133 STO3 171 RCL6 209 0 0 020 ÷ 058 — 096 RCLD 134 RCL5 172 + 210 X 021 RCL7 059 → P 097 + 135 RCL4 173 → P 211 PRTX 022 RCL5 060 X ≠ Y 098 → P 136 2 174 X ≠ Y 212 P ≠ S 023 X 061 RCL3 099 X ≠ Y 137 ÷ 175 PRTX 213 RTN 024 TAN 062 + 100 CHS 138 → R 176 X ≠ Y 214 LBLB 025 X 063 STO1 101 STO7 139 STO4 177 LOG 215 STOD 026 — 064 X ≠ Y 102 X ≠ Y 140 X ≠ Y 214 LBLB 025 X 063 STO1 101 STO7 139 STO4 177 LOG 215 STOD 026 RCLB 066 X 104 STOB 142 RCL7 180 X 218 CHS 067 SCLB 103 RCLA 027 STOA 065 RCL2 103 1/X 141 STO5 179 0 217 X 028 RCLE 066 X 104 STOB 142 RCL7 180 X 218 CHS 033 RCL7 221 RCLB 067 STOO 105 RCLB 143 RCL6 181 PRTX 219 1 030 RCL2 068 P ≠ S 106 RCLC 144 → R 182 RCL3 220 + 031 ÷ 069 RCLB 107 — 145 STO6 183 RCL7 221 RCLB 032 RCL1 070 RCL6 108 RCLA 146 X ≠ Y 184 — 222 ÷ 033 RCL7 071 ÷ 109 RCLD 147 STO7 185 RCL2 223 STOC 034 X 073 RCL5 111 → P 149 RCL5 187 — 035 TAN 073 RCL5 111 → P 149 RCL5 187 — 036 X 2 24 RTN 035 TAN 073 RCL5 111 → P 149 RCL5 189 X ≠ Y 037 — 075 TAN 113 RCL7 151 RCL0 189 X ≠ Y	009	RCL3	047	$X \rightleftharpoons Y$	085	RCL7	123	÷	161	+	199	-
012 COS	010	X	048	CHS	086	×	124	→R	162	1	200	RCL0
013 STOE	011	ENT↑	049	STO3	087	TAN	125	STO0	163	RCL9	201	RCL4
014	012	COS	050	$X \rightleftharpoons Y$	088	÷	126	$X \rightleftharpoons Y$	164		202	
015 SIN	013	STOE	051	1/X	089	+	127	STO1	165	÷	203	→P
016 RCL4 054 RCLC 092 RCLB 130 →R 168 RCL7 266 X ≠ Y 017 X 055 → 093 RCLC 131 STO2 169 + 207 LOG 018 STOB 056 RCLA 094 + 132 X ≠ Y 170 RCL2 208 2 019 RCL6 057 RCLD 095 RCLA 133 STO3 171 RCL6 209 0 020 ÷ 058 → 096 RCLA 133 STO3 171 RCL6 209 0 X 021 RCL7 059 →P 097 + 135 RCL4 173 →P 211 PRTX 022 RCL5 060 X ≠ Y 098 →P 136 2 174 X ≠ Y 212 P ≠ S 023 X 061 RCL3 099 X ≠ Y 137 ÷ 175 PRTX 213 RTN 024 TAN 062 + 100 CHS 138 →R 176 X ≠ Y 214 *LBLB 025 X 063 STO1 101 STO7 139 STO4 177 LOG 215 STOD 026 → 064 X ≠ Y 102 X ≠ Y 140 X ≠ Y 178 2 216 RCLA 027 STOA 065 RCL2 103 1/X 141 STO5 179 0 217 X 028 RCLE 066 X 104 STO6 142 RCL7 180 X 218 CHS 029 RCLB 067 STO0 105 RCLB 143 RCL6 181 PRTX 219 1 030 RCL2 068 P ≠ S 106 RCLC 144 →R 182 RCL3 220 + 031 † 069 RCLB 107 → 145 STO6 183 RCL7 221 RCLB 032 RCL1 070 RCL6 108 RCLC 144 →R 182 RCL3 220 + 031 † 069 RCLB 107 → 145 STO6 183 RCL7 221 RCLB 032 RCL1 070 RCL6 108 RCLC 144 →R 182 RCL3 220 + 031 † 069 RCLB 107 → 145 STO6 183 RCL7 221 RCLB 032 RCL1 070 RCL6 108 RCLC 144 →R 182 RCL3 220 + 031 † 069 RCLB 107 → 145 STO6 183 RCL7 221 RCLB 032 RCL1 070 RCL6 108 RCLC 144 →R 182 RCL3 220 + 031 † 069 RCLB 107 → 145 STO6 183 RCL7 221 RCLB 032 RCL1 070 RCL6 108 RCLA 146 X ≠ Y 184 → 222 † 033 RCL7 071 † 109 RCLD 147 STO7 185 RCL2 223 STOC 034 X 072 RCL7 110 → 148 RCL1 186 RCL6 224 RTN 035 TAN 073 RCL5 111 →P 149 RCL5 187 → 1036 X 974 X 112 X ≠ Y 150 + 188 →P 037 → 075 TAN 113 RCL7 151 RCL0 189 X ≠ Y	014	$X \rightleftharpoons Y$	052	STO2	090	GSBB	128	RCL3	166	PRTX	204	$X \rightleftharpoons Y$
017	015	SIN	053	RCLB	091	$P \rightleftharpoons S$	129	RCL2	167	RCL3	205	PRTX
018 STOB	016	RCL4	054	RCLC	092	RCLB	130	\rightarrow R	168	RCL7	206	$X \rightleftharpoons Y$
019 RCL6 057 RCLD 095 RCLA 133 ST03 171 RCL6 209 0 020 ÷ 058 − 096 RCLD 134 RCL5 172 + 210 X 021 RCL7 059 →P 097 + 135 RCL4 173 →P 211 PRTX 022 RCL5 060 X ⇌ Y 098 →P 136 2 174 X ⇌ Y 212 P ⇌ S 023 X 061 RCL3 099 X ⇌ Y 137 ÷ 175 PRTX 213 RTN 024 TAN 062 + 100 CHS 138 →R 176 X ⇌ Y 214 *LBLB 025 X 063 ST01 101 ST07 139 ST04 177 LOG 215 ST0D 026 − 064 X ⇌ Y 102 X ⇌ Y 140 X ⇌ Y 178 2 216 RCLA 027 ST0A 065 RCL2 103 1/X 141 ST05 179 0 217 X 028 RCLE 066 X 104 ST06 142 RCL7 180 X 218 CHS 029 RCLB 067 ST00 105 RCLB 143 RCL6 181 PRTX 219 1 030 RCL2 068 P ⇌ S 106 RCLC 144 →R 182 RCL3 220 + 031 ÷ 069 RCLB 107 − 145 ST06 183 RCL7 221 RCLB 032 RCL1 070 RCL6 108 RCLA 146 X ⇌ Y 184 − 222 ÷ 033 RCL7 071 ÷ 109 RCLD 147 ST07 185 RCL2 223 ST0C 034 X 072 RCL7 110 − 148 RCL1 186 RCL6 224 RTN 035 TAN 073 RCL5 111 →P 149 RCL5 187 − 036 X 074 X 112 X ⇌ Y 150 + 188 →P 037 − 075 TAN 113 RCL7 151 RCL0 189 X 록 Y			055	-	093	RCLC	131	STO2	169	+	207	LOG
020 ÷ 058 − 096 RCLD 134 RCL5 172 + 210 × 021 RCL7 059 →P 097 + 135 RCL4 173 →P 211 PRTX 022 RCL5 060 X ≠ Y 098 →P 136 2 174 X ≠ Y 212 P ≠ S 023 X 061 RCL3 099 X ≠ Y 137 ÷ 175 PRTX 213 RTN 024 TAN 062 + 100 CHS 138 →R 176 X ≠ Y 214 *LBLB 025 X 063 STO1 101 STO7 139 STO4 177 LOG 215 STOD 026 — 064 X ≠ Y 102 X ≠ Y 140 X ≠ Y 178 2 216 RCLA 027 STOA 065 RCL2 103 1/X	018	STOB	056	RCLA	094	+	132	$X \rightleftharpoons Y$	170	RCL2	208	2
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$\begin{array}{cccccccccccccccccccccccccccccccccccc$	022	RCL5	060	$X \rightleftharpoons Y$	098	→P	136	2	174	$X \rightleftharpoons Y$	212	P ⇒S
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$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		X	063	STO1	101	STO7	139	STO4	177		215	STOD
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		-	064	$X \rightleftharpoons Y$	102	$X \rightleftharpoons Y$	140	$X \rightleftharpoons Y$	178	2	216	RCLA
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036 X 074 X 112 X \rightleftharpoons Y 150 + 188 $→$ P 037 - 075 TAN 113 RCL7 151 RCL0 189 X \rightleftharpoons Y			2000 200	100/10/10/10/10		-			0.00	RCL6	224	RTN
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		×				$X \rightleftharpoons Y$			188	→P		
038 GSBB 076 ÷ 114 + 152 RCL4 190 PRTX		_										
	038	GSBB	076	÷	114	+	152	RCL4	190	PRTX		Control of the

Instructions

- Key in program
- Enter normalized frequency and coupler's parameters
 (f/f₀), STO 0, (a₁), STO 1, (z₁), STO 2, (a₂), STO 3, (z₂), STO 4, (a₃), STO 5, (z₃), STO 6
- Press R/S
 Normalized frequency (f/f₀), phase and amplitude of reflection coefficient at input (φ₁, |Γ₁|), VSWR at input (S), phase and amplitude of wave at second, third, and fourth arms of coupler (φ₂, A₂, φ₃, A₃, φ₄, A₄) are displayed
- Enter new normalized frequency to generate corresponding phase and amplitude information (f/f_n), R/S

seen in (a). Here A, B, C, and D are proportionality factors corresponding to the particular network analyzed. Further, it can be shown that when networks in the microwave region are considered, values A through D are specified by analyzing the black box as a transmission line flanked by two stubs at each end, where z_1 and l_1 , and z_3 and l_3 , are the normalized impedance and length of the two stubs. Impedance z_2 and length l_2 correspond to the transmission-line parameters. Each section has a matrix, and when they are multiplied together, they equal the matrix of the proportionality factors A-D.

If a symmetrical coupler is analyzed and assumed to be lossless, then the matrix equation can be written as shown in (b), where $a_i = 4l_i/\lambda$, $\theta = 90f/f_o$, $\gamma = j\beta$, and $\beta l_i = a_i\phi$. The HP-97 will solve these matrices for any symmetrical coupler.

The illustration shows the results of a plot carried out for one of the most popular coupler configurations now available, where $a_1 = 0.5$, $a_2 = 1.0$, $a_3 = 1.5$, and normalized impedance values are $z_1 = 2^{1/2}$, $z_2 = 2^{1/2}$, and $z_3 = 2^{1/2}$. Entering these values into the calculator as instructed will generate information in tabular form for each normalized frequency desired.

Engineer's newsletter.

New to laser trimming? Try contracting it out

Thinking of buying a \$250,000 to \$500,000 laser trimmer? Perhaps you should look into an alternative—contract laser trimming. Laser Trim Inc. has the equipment to trim thick- or thin-film resistor networks to a ratio accuracy of 0.002% at rates of up to 50,000 units per hour.

Contract trimming also provides an easy transition for those about to buy a laser system. Laser Trim can work out all the trimming problems, tooling, and programs before a user purchases his own trimmer and pass all this material along to him when his machine arrives—a procedure that is bound to make life easier for a first-time user. More information is available from the company at 4009 North Nashville, Chicago, Ill. 60634.

Another use for a microprocessor's restart command

Included in the repertoire of several microprocessors are one or more software interrupt instructions. The chief function of this kind of instruction is to transfer control to an interrupt routine when the appropriate op code is forced onto the data bus by an internal device's request for service. Because it carries an implied vector, the software interrupt minimizes the code that must be directed into the processor.

The eight restart instructions common to the 8080, 8085, and Z80 are good examples. Bernard Verreau of Intel's Microcomputer Systems division points out that these "RST O, . . . 7" instructions can also be used as unconditional subroutines to call in an assembly language program. They offer the dual advantage of faster execution and fewer bytes than the standard call instruction. In fact, if the most frequently referenced subroutines are accessed through restarts, a substantial memory saving may result.

It pays to pay more on packaging optical devices

Shipping optical laser components is not a simple procedure, as a Government laboratory that uses many of these delicate and costly elements found, to its expense. It came to Zero Corp., in Burbank, Calif., for help with its problem—the marring and staining of the optical surfaces of laser components, mainly lenses, which it had been shipping all over the world in plastic or wooden boxes containing polyurethane packing.

Zero's solution was an aluminum carrying case fitted with a customdesigned polyethylene insert. The case protects its contents against shock and vibration, while the tongue-and-groove design of the shell plus a neoprene gasket excludes outside elements like rain, snow, or excessive humidity. Also, unlike the boxes, the aluminum case is reusable.

Chip monitors power supply

Most power supplies require additional circuitry for monitoring their performance and protecting them in the event of a fault. An application note from Silicon General Inc. describes an interesting new monolithic integrated circuit that contains all the functions necessary to monitor and control the output of any power supply system. Called "The Output Supervisory Circuit," the note also suggests applications for the new chip, including limiting linear foldback, sensing multiple supply voltages, and overcurrent, undervoltage, and overtemperature shutdown. To receive a copy, write to the company at 11651 Monarch Street, Garden Grove, Calif.

—Jerry Lyman

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free-for-the-asking catalog: Low level amplifiers — differential amplifiers — level detectors — DC to DC converters — timing circuits — motor speed controls — optical detector systems — camera controls — plus, flip chips.



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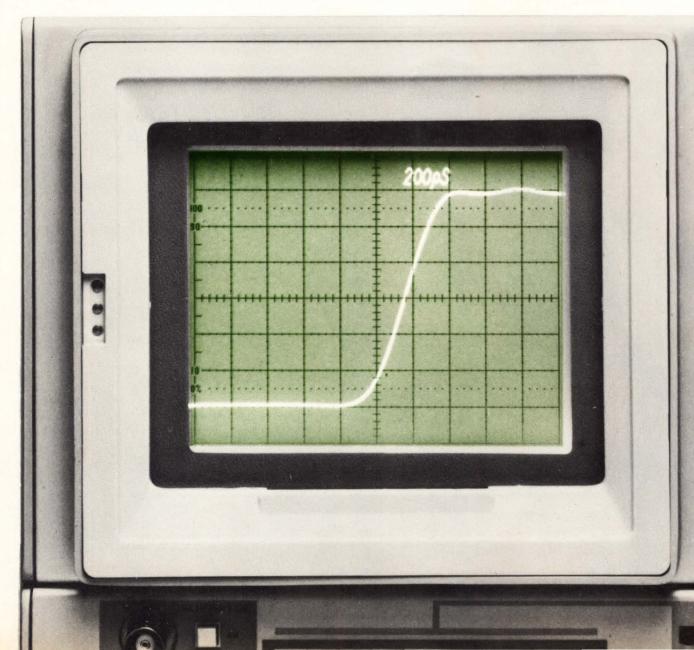
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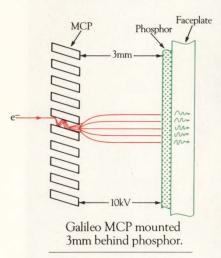
On the long road Tektronix

As a result of the meeting, events never before seen by the naked eye came to light on Tektronix' new 7104—the world's fastest general purpose oscilloscope. Events such as a pulse with the incredibly short rise time of 350 picoseconds. To follow such fleeting

excursions, the beam energy had to be low enough to be steerable—so low, in fact, that the phosphor couldn't light up. All of Tektronix' innovations in high speed circuitry might have come up against laws of physics: Too few electrons to produce visible photons.

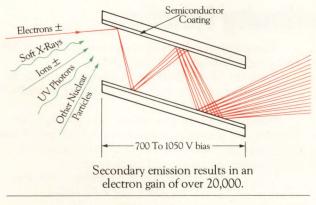


to1GHz, met Galileo.



So Tektronix talked with Galileo, because we pioneered the development of electron multiplier arrays called Micro-Channel Plates. Positioned just behind the phosphor surface in the CRT, our MCP delivers 20,000

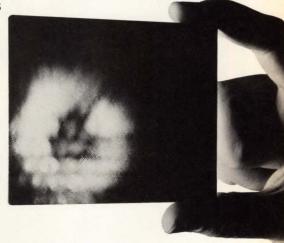
times more electrons to the phosphor surface than it receives from the weak beam. The resulting trace is almost 1000 times brighter enough to be seen easily and recorded with conventional photographic techniques and film.



As you can see, Tektronix' solution was based not on brute-force engineering but on imaginative use of advanced technology. At Galileo this technology arises from a unique blend of applied physics and glass making. The MCP has found applications in mass and vacuum UV spectrometers, fusion and other energy-related detection systems, elec-

tron and ion microscopes, electron beam lithography, and in nuclear and medical research. MCP's are available in various

sizes, shapes and geometries to meet your requirements. In addition, Galileo is the world's largest manufacturer of singlechannel electron



multipliers for use in a wide variety of atomic particle and photon detectors.

Tektronix' application involved electrons. It could just as easily have been a success story about ions, protons, soft X-rays, beta particles, vacuum UV photons, or metastable particles. The application might be in counting, mapping, or imaging. The possibilities for dramatically improving the performance of an industrial product with Galileo technology are wide open to any imaginative designer, including you.

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BECKMAN

Tester for bubble memories first in field

System is designed for engineering and production and can handle variety of devices in package or wafer

by Robert Brownstein, San Francisco regional bureau

The ten-year trek from laboratory to production line is now a part of bubble-memory history. Commercial reproducibility is spurring manufacturers to develop and employ such products, so test-equipment makers are racing to gain an early lead in what could become a sizeable market [Electronics, March 29, 1979, p. 35].

The winner of the first lap appears to be Megatest Corp., which is not, as might be expected, one of the test industry giants, but a small Santa Clara company. Its product, succinctly named the bubble-memory test system, addresses both the engineering shop and the production line.

This duality of purpose is not a "value-added ploy" but a marketing necessity, claims Steve Bisset, president of Megatest. The operational characteristics of bubble memories make testing a long process. Furthermore, Bisset points out, "Bubbles are new, so testing is going to involve a lot of analysis." Megatest's designers feel they have covered all bases by providing a proprietary pattern processor and offering the option of testing up to eight devices in parallel.

To accommodate a great variety of test conditions, the memory's bubble-propagating drive field, its gating loops, and its bias field must be independently controlled. To note the presence of a magnetic bubble, the system must be able to measure a flea-sized magnetoresistive distortion in its permalloy detector. What is therefore required in such a tester is hardware that provides programmable currents up to tens of amps, is fast, and can sense extremely low-level signals.

To be versatile, the hardware must have a controller that directs it, collects and stores the data it provides, and is easy to program. The Megatest system incorporates all these hardware and controller features. In addition, it can even be tied to a host computer for large-scale distributed processing.

The system is divided into three parts: a PDP 11/V03 central processing unit with dual floppy-disk drives, a tall rack containing analog and digital hardware, and a test head to accept either packaged devices or wafers.

Programmers at the PDP 11 terminal will work in an extended version of Pascal. It includes structures to ease parameter specification plus simple commands for displaying test results, mapping bad loops, and logging results on disk. Software breakpoints are provided for debugging and utilities are included for constructing shmoo plots and histograms.

Most bubble devices available now (and those that will be shortly) use block-replicate or major-minor loop architecture. From type to type, the organization of magnetic bubbles to represent a given block of data varies. The relative position of these bubbles from one loop to the next, referred to as the device's topology, can affect the memory's operation.

Megatest's engineers decided that letting a pattern processor handle device topology would make writing programs for more than one vendor's devices considerably easier. A byproduct, Bisset claims, is that it helps push throughput way up.

The pattern processor contains a sequence controller, an image con-

troller, and an error-map memory. Both the image controller and the error map are organized topologically. At the behest of the sequence controller, the image controller will write or read a block of data arranged in accordance with the architecture of the chip under test. The sequence controller is arranged in terms of events and oversees the order of read, write, transfer, and block move operations.

Both controllers orchestrate the timing generator, which uses emitter-coupled logic for speed. The generator, in turn, controls the timing of signals emanating from the current pulsers and the drivers for the drive-field and the bias-field coils.

Various parameters of the drivers and pulsers—such as magnitude, phase, and pulse width—are digitally controlled by the PDP 11's CPU





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Circle 238 on reader service card

The right angle is the right idea.

C&K's right angle miniature toggle switch mounts directly on P.C. boards with a low

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Circle 168 on reader service card

via the data bus. The CPU presets various parameter values digitally, but it is the pattern processor which synchronizes and controls the changes on the drivers' outputs.

Programmable X and Y voltages of the tester's drive-field coil driver determine the peak current supplied to that coil of the memory. For packaged devices, they can be specified in 10-mv steps over a 0-to-30-v range to an accuracy within 50 mv. The resultant output current peak can be a maximum of 3 A with a 1-A average at the upper frequency limit of 500 kHz.

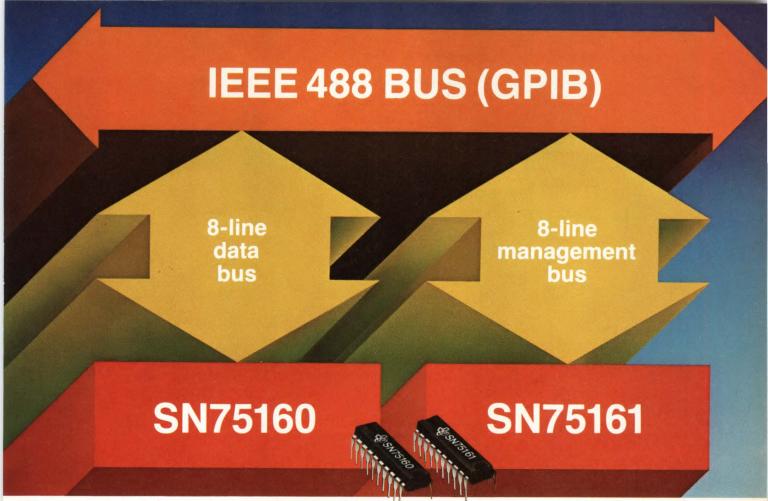
For probing wafers, the tester has circuitry to drive field coils in the wafer fixture. This requires more power than a package's coils use and, therefore, it can drive ±16 A, peak, with 75-V compliance at a maximum frequency of 300 kHz.

To detect the presence of a bubble, a sampling of voltage is taken at two intervals during which a bubble could be passing under a permalloy chevron detector. A constant current is fed into the actual detector and a second, dummy detector. The voltage drop produced is sampled differentially to eliminate variations due to rotating field effects.

Nucleating (forming) a bubble, transferring it, replicating it, or annihilating it is done by controlling the phase, width, and magnitude of gating pulses. Six drivers are provided; each has a 0.5-ma resolution over a 0-to-250-mA range with accuracy to within 2% ±5 mA. Rise and fall times are 25 ns and voltage compliance is variable between 0 and 30 v. All pulsers are short-circuit protected and up to 20 can be accommodated by the system.

Megatest's system ranges in cost from \$90,000 up to \$125,000 with available options like a printer, second test head, rigid disk drive, extra pulsers, and others. Delivery will begin by the end of May, Bisset says, and first systems are slated to go to Rockwell's Electronic Devices division in Anaheim, Calif.

Megatest Corp., 2900 Patrick Henry Dr., Santa Clara, Calif. 95050. Phone (408) 988-1700 [338]



Reduce power and board space 40%. TI's new octal transceivers.

Introducing two new octal, bidirectional bus transceivers that meet the IEEE 488 General Purpose Interface Bus (GPIB) Standard.

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The SN75160 and SN75161 feature:

- Built-in bus terminating resistors on driver outputs
- High impedance to bus during power down
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- 3-state outputs on receiver
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- High impedance PNP inputs
- 20-pin dual-in-line package

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equipment on a bi-directional 8-

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protocol to assure interlocked

communication between talker

In 100 pieces, the cost for SN75160 is \$3.90. The 100 piece

authorized TI distributor. For data sheet information write: Texas Instruments Incorporated, P.O. Box 225012, M/S 308, Dallas, Texas 75265.

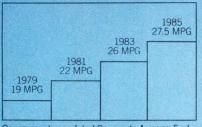
TEXAS INSTRUMENTS

INCORPORATED

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MOTOROLA HELPS STRETCH GAS MILEAGE

Automotive manufacturers are caught between a rock and a hard place. They are obliged not only to reduce fuel consumption, but also, at the same



Government mandated Corporate Average Fuel Economy (CAFE) standards. Source: NHTSA

time, to reduce harmful exhaust gas emissions. And these objectives seem to be mutually exclusive.

An engine whose carburetor and spark timing are

adjusted to give high mileage tends to produce unacceptable levels of pollution. The same engine, adjusted for low pollution levels, uses more gas and gives disappointing performance.

The trick is to burn exactly the right amount of fuel at exactly the right moment. But what is "right" depends on a whole complex of constantly changing factors, including terrain, engine and air temperature, barometric pressure, and the load and speed of the car.

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It's a real computer in



BY MAKING ENGINES THINK.

miniature, with a memory and the ability to manipulate what it learns in terms of what it already knows. It works so well that car and heavy-duty-equipment manufacturers in America and Europe plan to use it, some as early as the 1980 model year.

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Such precise, continuous engine management would be impossible without the integrated circuit, an electronic microcosm that contains the equivalent of twelve thousand transistors and measures about 5mm square. These small miracles are the central nervous system of Motorola's electronic engine-management system,

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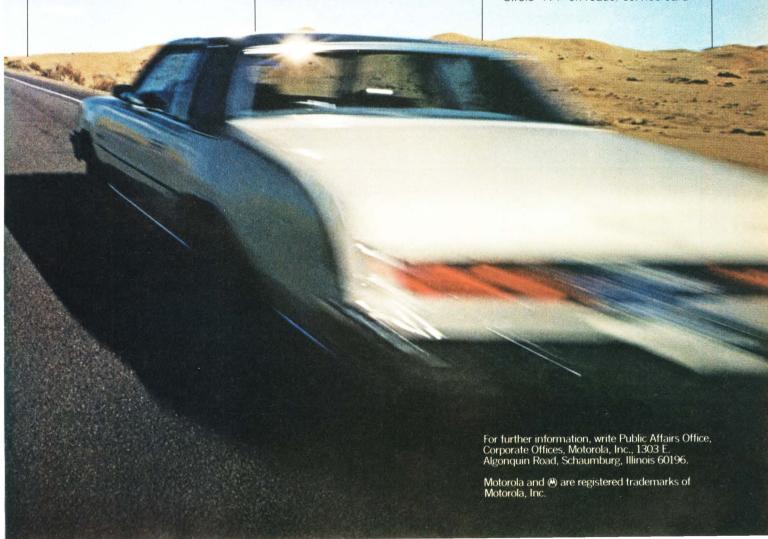
We make microelectronics carry telephone services to places where there are no phone lines. Transmit electrocardiograms and voice messages simultaneously from the scene of an accident to a nearby hospital. Help the energy industries develop the resources of the earth, the sea and the sun.

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W MOTOROLA

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Circle 171 on reader service card



Op amps give more for less

Dual devices for audio and for video applications demonstrate the op amp's ability to perennially challenge engineering creativity

by William F. Arnold, San Francisco regional bureau manager, and Nicolas Mokhoff, Components Editor

Of all the circuits an engineer encounters, the one that never seems to lose its appeal is the operational amplifier. Simple and easy to use, it nonetheless challenges his inventiveness. These observations are borne out by the LM13600 and the LM359. Created from earlier models, the two low-cost devices extend the applicability of op amps.

The LM3080 operational amplifier, a transconductance type that puts out current for a voltage input, is well suited for use in electronic organs and music synthesizers because it easily modulates waveshapes. Then National Semiconductor Corp. began wondering how it could improve things.

First, it found that it could put two amplifiers on one chip, which would improve circuit density and not use up all the pins in a 16-pin package, recalls Tim D. Isbell, director of consumer linear integrated circuit design. "Okay, what can I do with the rest of those pins?" he then mused. What he found he could do was add on-chip Darlingtons, so users could buffer the outputs, and linearizing (or Gilbert) diodes on the inputs, so they could accept higher-level signals while reducing distortion (a 10-dB signal-to-noise ratio improvement referred to 0.5% total harmonic distortion).

The result is the LM13600 dual operational transconductance amplifier, which National believes has wide applications, not only in audio equipment, but in a variety of industrial and process-control systems. These applications include current-controlled amplifiers, filters, and oscillators as well as multiplexers, timers, and even sample-and-hold circuits. In some cases, the LM13600 could replace mechanical potentiometers and act under the control of a microcomputer in indus-

trial process-control systems.

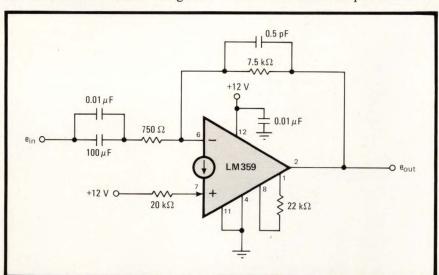
In the LM13600, the two transconductance amplifiers share common supplies but otherwise act independently, with individual differential inputs and push-pull outputs. National also says that the device has excellent matching between the amplifiers. The supply range is wide: ± 2 to ± 20 v.

Interesting. For the designer, the LM13600 has these interesting specifications. The common-mode rejection ratio over the common-mode input range of ± 12 V is 80 dB minimum, with 110 dB typical. Input offset voltage is typically 0.4 mV, input offset current is typically 0.1 mA, and input bias current is typically 0.4 mA.

Transconductance is 5,400 micromhos, or rather microsiemens (abbreviated μ S) minimum for the part with a 0-to-70°C range and 4,000 μ S minimum for the device with a range of -55° to $+125^{\circ}$ C. Both parts show a typical transconductance tracking figure of 0.3 dB. Maximum leakage current is 100 nA and only 5 nA, respectively.

For applications, Isbell points to various circuit configurations. For example, as a voltage-controlled oscillator, the LM13600 can be implemented in function generators, organs, and process-control systems. It also can be designed into a battery powered sensing instrument so that it would turn on periodically to detect any presence of gas but remain off in between. In all, National lists 31 applications for the LM13600. Both versions cost \$1 each in high volume.

Take the popular LM3900 quad op amp, slice it in half, and increase



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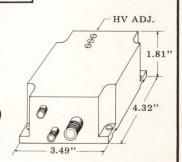
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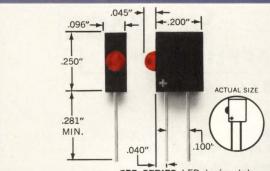
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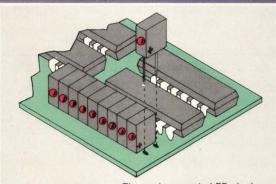




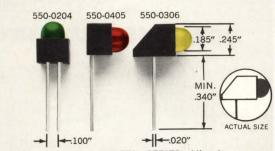
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Circle 174 on readerservice card

New products

the unity-gain bandwidth from 2.5 to 30 MHz. The result is a dual video amplifier called the LM359.

Projecting its original concept into the video arena, National hopes to give a totally different perspective to users who need broadband amplification, fast slew rate, and stable operation with a closed-loop gain of 10 or better. At gains from 10 to 100, the gain-bandwidth product is 400 MHz and slew rate is 60 V/µs (at unity gain, the slew rate is 30 V/µs).

"The significant improvement in frequency response is the result of using a common-emitter/commonbase, or cascode, gain stage," explains Nello Sevastopoulos, standard linear IC applications section head.

Another important feature is the current-mirror configuration, he adds. To work as it does from a single supply, the output must have a dc bias. "The current-mirror feature facilitates this task by always having both the ac and dc currents that flow into the noninverting input force an equal amount of current to flow into the inverting input," he says. Placing a reference dc current on the positive input and making the output drive the negative input forces the output dc level to the value needed.

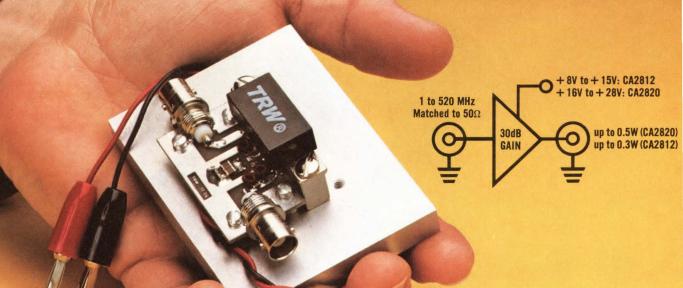
The product can be externally programmed to suit a wide variety of applications. Besides general-purpose color video amplification, these include such uses as high-frequency, high-Q active filters, photodiode amplifiers, and waveform generation circuits with a video frequency range. The amplifiers, like the LM13600, work from a wide power range, in this instance +5 to +22 v. They can accommodate input common-mode voltages greater than the supply voltage.

The open-loop voltage gain of the device is 72 dB at a supply voltage of +12 V and a l-k Ω load at a frequency of 100 Hz. Maximum power dissipation is a hefty 1 W. The LM359, a 0°-to-70° device, costs \$1.50 in 100s and is available from stock.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Circle reader service number 339 for the LM13600, 341 for the LM359.

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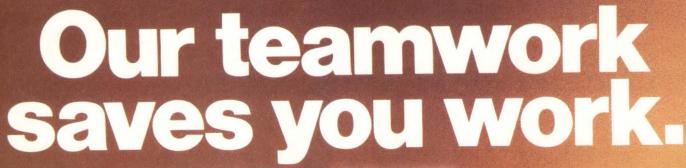
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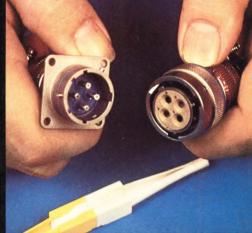
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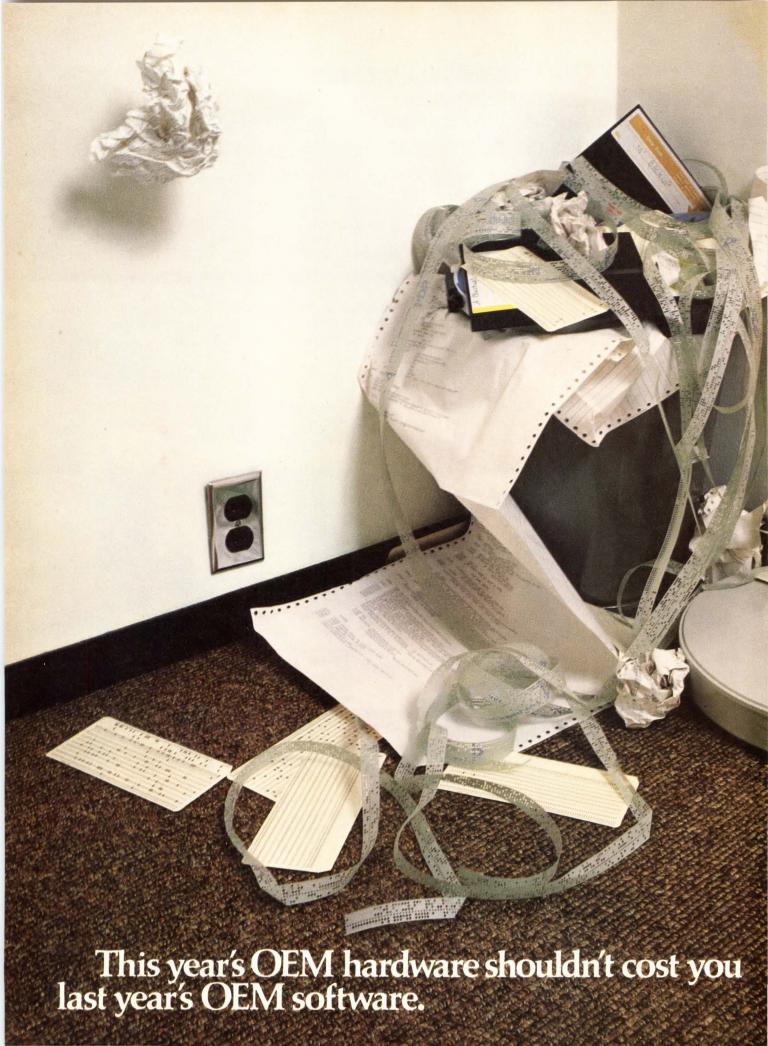


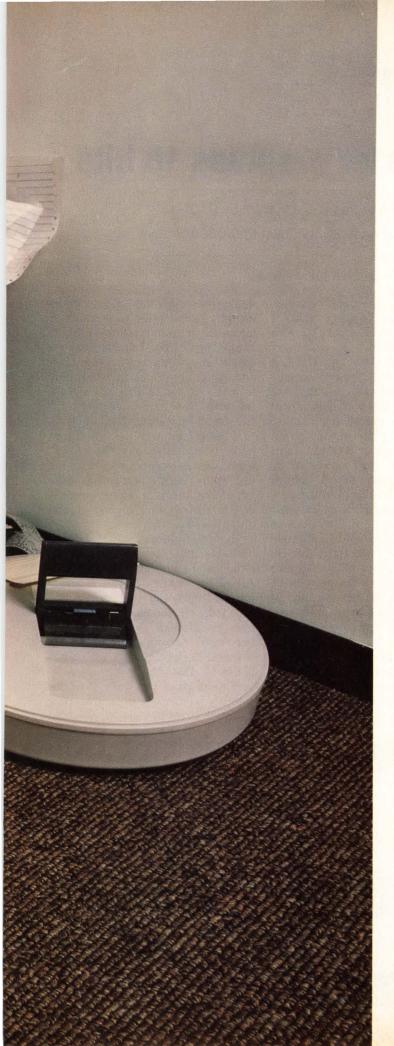


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Hybrid d-a converter resolves 18 bits

Housed in a 32-pin DIP that measures 1.77 by 1.15 by 0.22 in., high-accuracy device keeps nonlinearity down to 0.0008%

by James B. Brinton, Boston bureau manager

Eighteen-bit digital-to-analog converters of any size are tough enough to find, but a hybrid unit is rare indeed. Just such a device, however, has just been introduced by Hybrid Systems Corp. Called the DAC 374-18, the unit packs 18-bit resolution, 0.0008% nonlinearity, as well as mil-spec performance into a 32-pin dual in-line package with dimensions of 1.77 by 1.15 by 0.22 in. Exactly how the feat was achieved, the world won't learn for a while because much of the design is secret, pending the filing of patent applications.

Samual Wilensky, vice president of the company, will go so far as to say that the new approach makes the converter almost totally insensitive to the characteristics of its internal switching network. "This DAC's accuracy is almost totally a function of its resistor network," he says, "and we are using thin-film laser-trimmed resistors. They are trimmed to extreme accuracy to begin with, and because they are all on a common glazed-silicon substrate, their ther-

mal tracking is quite tight." Guaranteed worst-case linearity drift is ± 2 parts per million per °C, with ± 1 ppm/°C typical.

The converter is not only small, it also dissipates little power—important because compact packages are often used in tight layouts where minimizing the overall temperature rise can be a problem. Its power requirement is about 500 mW, compared with the 1 to 2 W needed by competing modules. Supply voltage is ±15 V; no 5-V supply is required.

Also not required is an external voltage reference; a -10-v reference is built in. The unit will accept external references if necessary though, and in some ultra-close-tolerance applications this probably will be necessary since the performance of the built-in reference limits the performance of the converter. Its drift is about ±5 ppm/°C maximum, ±3 ppm typical.

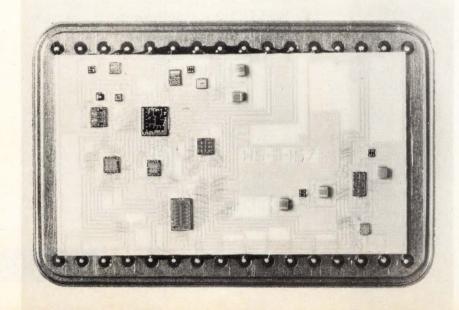
The converter accepts unipolarbinary and bipolar-offset-binary inputs from transistor-transistor, diode-transistor, and 5-V complementary metal-oxide-semiconductor logic. Its output is 0 to \pm 10 V, \pm 5 V, or \pm 10V. The unit has an output impedance of less than 1 Ω and can deliver 2 mA. Settling time to within 0.05% of final value, for a full-scale 10-V output change, is 50 μ s—faster than some 16-bit units.

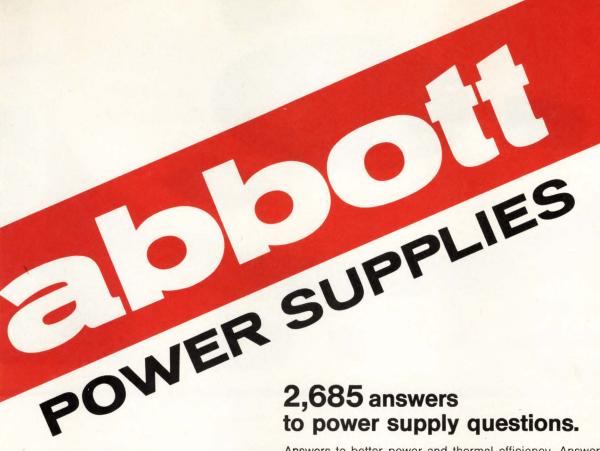
Wilensky expects the 374-18 to find its way into many "insurance" applications—situations in which the user really needs 16-bit performance but doesn't trust a 16-bit converter—as well as into high-resolution displays and references.

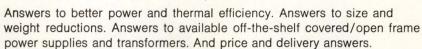
Hybrid Systems is a qualified MIL-M-38510 supplier that routinely builds products to MIL-STD-883. All of its DAC 374-18s, whether intended for military use or not, will be made on the same production lines up through the visual-inspection step. According to marketing manager G. James Estep, the principal factor that then makes the military units more expensive than the commercial ones is documentation. In small quantities, the commercial version goes for \$350, whereas a similar converter qualified to MIL-STD-883, Class B goes for about \$725. At the 100-unit level, these prices drop to \$260 and \$520, respectively. MIL-M-38510 parts will also be offered, but at a somewhat higher price.

Interestingly, these prices also are highly competitive. Similar devices housed in modules typically sell from about \$640 to more than \$1,100. Delivery time for the DAC 374-18 is 10 to 12 weeks.

Hybrid Systems Corp., Crosby Drive, Bedford, Mass. 01730. Phone (617) 275-1570 [340]







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Transformer Catalog — We specialize in custom transformers, and this 20-pager gives you detailed information on how to specify for your exact requirements. It also covers over 800 standard military, industrial and miniature pcb transformers, including 60 and 400Hz, single phase input units. Prices for standards start as low as \$5.10 for up to 9 pieces.

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See Power Supply Section 4000, and Transformer Section 5600, Vol. 2, of your EEM catalog; or Power Supply Section 4500, and Transformer Section 0400, Vol. 2, of your GOLD BOOK for complete information on Abbott products.

abbott transistor

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Store Recorders have made



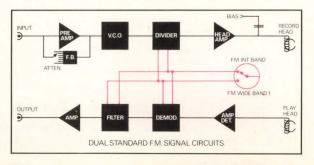
Flick a single switch on a dual standard recorder in the new Racal Store DS range, and you've changed instantly from Intermediate Band to Wideband operation on FM. A single switch that selects either recording standard – without the need to interchange plug-in modules. A single switch changes all the signal channels (four to fourteen) on all seven speeds.

FM Capability

The Store range of instrumentation recorders, well-renowned for research in the scientific, automobile, aerospace and medical fields, now offers an FM capability over the entire band DC to 40 kHz, and up to 300 kHz on Direct Recording.

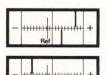
Greater Flexibility

And even greater flexibility. Switch any channel to unipolar, and the full dynamic range becomes available to either positive or negative going signals. Switch any channel to offset, and you can record a 100 mV peak-to-peak signal on a 20 V step—without losing any dynamic range.





a quick switch to wideband.



Proven Success

All these outstanding new advantages have been added to the host of features which have made the existing range such a success—like single switch seven-speed selection, full servo operation, dual peak-indicating meters, full remote control of all functions, portability, and operation

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That's why, by switching to the Racal Recorders' new Store DS range, you can make a quick switch to a whole new wideband world.

Racal Recorders Limited Hardley Industrial Estate, Hythe Southampton Hampshire SO4 6ZH England Telephone: 0703-843265 Telex: 47600.

Racal Recorders Inc 5 Research Place, Rockville Maryland 20850, Telephone: (301) 948 3085.

Racal Recorders Inc, 1109 West San Bernardino Road, Suite 110 Covina California 91722 Telephone: (213) 967 2869.

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These remarkable agents improved processability through reduced viscosity, faster wetting and better dispersion. And helped improve moisture resistance, barrier properties and everything from better

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To learn about hundreds more, please write to us at Dept. JSW. 270 Park Avenue, New York, N.Y. 10017. Just describe your system and the properties you want. We'll be glad to recommend the correct silane coupling agent as well

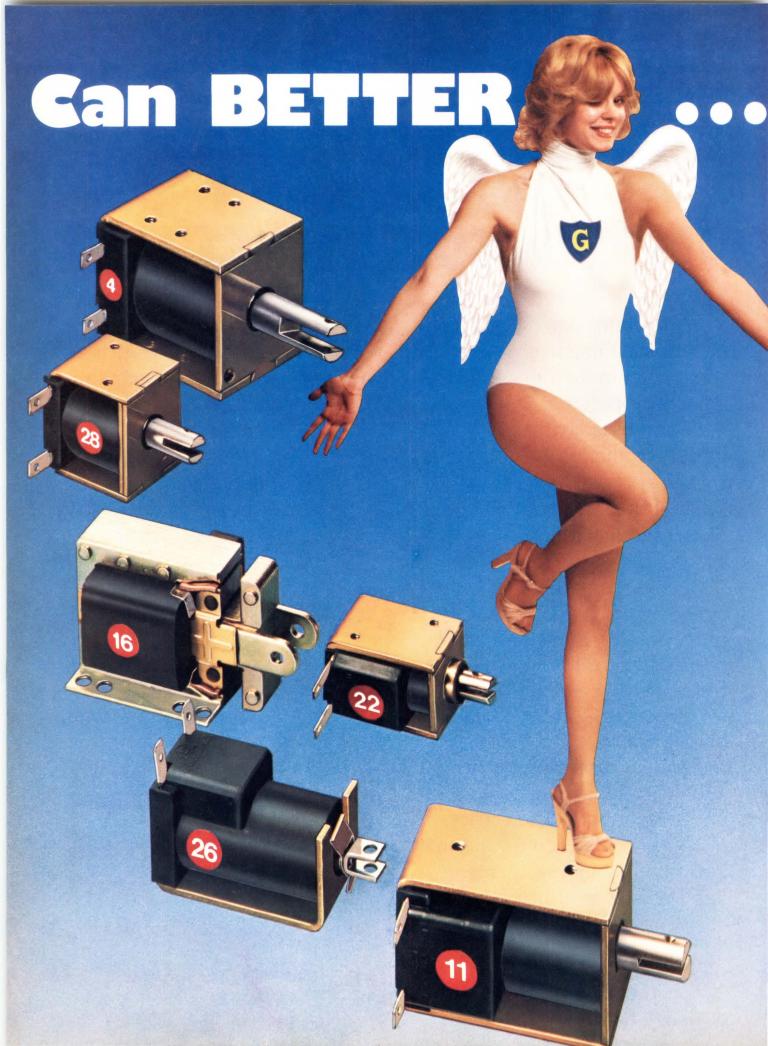
Foundry-cast engine block 2. Tires 3. Grill-

1. Foundry-cast engine block. 2. Tires. 3. Grillopening, header panels. 4. Electric guitar case. 5. Golf-ball core. 6. Fiberglass skis. 7. Home insulation. 8. TV circuit board. 9. Telephone circuit board. 10. Fiberglass curtains. 11. Trouble-light EPDM insulation. 12. Hand-drill housing. 13. Fiberglass boat. 14. Roof shingles.

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Your Guardian Angel has a solenoid bargain for you. Solenoids that are ready for immediate delivery at important savings. The six solenoids used most in applications like yours. The ones we stock in depth for instant shipment. The ones that save you so much it actually pays you to design them into your product. Or, to modify your mounting arrangement or other minor design elements to fit these stock solenoids. Because, when you order any of these solenoids, you save 12 to 15%!

All six of the Guardian best-sellers feature either Uni-Guard® II molded bobbin and coil covers or molded coils that give longer life—up to 5 million operations for most . . . 250,000 operations for the No. 16. All are pull type. All meet or surpass U/L and CSA component recognition requirements. All have .187" QC lug termination.

Guardian Number	Overall Dimensions	Coil Voltage	Duty	Power Ratin Minimum Stroke	ngs @ 25°C. Maximum Stroke
No. 4 Box Frame	2½6" x 1½6" x 1%"	120 AC 120 AC 24 DC 24 DC	Inter. Cont. Inter. Cont.	36 oz. at 1/8" 8 oz. at 1/8" 115 oz. at 1/8" 63 oz. at 1/8"	26 oz. at 1" 7 oz. at 1" 16 oz. at 1" 6 oz. at ½"
No. 11 Box Frame	1%" x 15/16" x 13/16"	120 AC 120 AC 24 DC 24 DC	Inter. Cont. Inter. Cont.	21 oz. at 1/8" 12 oz. at 1/8" 40 oz. at 1/8" 24 oz. at 1/8"	11 oz. at ¾" 6 oz. at ¾" 6 oz. at ¾" 3 oz. at ¾"
No. 16 Laminated	1%" x 1¼" x 1½"	120 AC 120 AC	Inter. Cont.	110 oz. at 1/8" 63 oz. at 1/8"	28 oz. at ¾" 15 oz. at ¾"
No. 22 Box Frame	15⁄32" x 3⁄4" x 3⁄4"	120 AC 120 AC 24 DC 24 DC	Inter. Cont. Inter. Cont.	20 oz. at ½6" 12 oz. at ½6" 20 oz. at ½6" 12 oz. at ½6"	2 oz. at %" 1.7 oz. at %" 2 oz. at %" 1.7 oz. at %"
No. 26 U-Frame	1¾" x ²⁷ ⁄ ₃₂ " x 1¾ ₁₆ "	120 AC 120 AC 24 DC 24 DC	Inter. Cont. Inter. Cont.	32 oz. at ½6" 17 oz. at ½6" 46 oz. at ½6" 26 oz. at ½6"	4 oz. at %" 6 oz. at %" 4 oz. at %" 3 oz. at ½"
No. 28 Box Frame	1½" x 1½2" x 1¾6"	120 AC 120 AC 24DC 24DC	Inter. Cont. Inter. Cont.	40 oz. at 1/16" 24 oz. at 1/16" 40 oz. at 1/16" 25 oz. at 1/16"	7 oz. at ½" 5 oz. at ½" 3 oz. at ½" 2 oz. at ½"

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Terminal shows full page

Based on a Z80 processor, terminal displays 60 lines of 80 characters

In word- and data-processing applications, the typical 80-character-by-24-line format can lead too frequently to scrolling. So Ann Arbor Terminals devised the 6080-Compat.

A Z80-based cathode-ray-tube terminal, it displays a full typewritten page of data: 60 lines of 80 characters. The terminal includes a 15-inch non-glare screen using the P39 green phosphor for greater readability and minimal reader fatigue. The 72-key detachable keyboard generates the full 128-character ASCII set.

Also standard are a numeric pad and cursor control keys. All keys have automatic repeat, and up to 36 special-function keys may be installed at the buyer's option.

Upper- and lower-case characters are formed in a 7-by-7-dot matrix on a 10-by-10-dot field. Three character accents—blink, dim, and reverse-video—are also provided for highlighting. The cursor is displayed as a blinking field.

All commands and controls are entered through the keyboard. Commands include erase memory; cursor home, return, up, down, right, and left; set cursor position; and set character accent. Control functions are communications rate (110 to 19,200 b/s), input/output mode (local, full, or half-duplex), keyboard mode (teletypewriter or full ASCII), and display mode (roll or page).

Measuring only 15 in. wide by 14 in. high by 13.6 in. deep, the terminal is packaged in Ann Arbor's compact E-Case, which weighs only 33 lb. Since all connections are made inside the unit, no connectors protrude from the case, making the 6080-Compat suitable for desktop

installations. A switching-regulator power supply allows a wide range of operating-voltage levels, including overseas conventions.

Options include 50-Hz refreshing, bell, various combinations of carriage return and line feed, and current-loop interface. Prices begin at \$1,895. Delivery typically takes 12 weeks.

Ann Arbor Terminals Inc., 6107 Jackson Rd. Ann Arbor, Mich. 48103. Phone Sarah Freeman at (313) 769-0926.

Controller colors communications conditions

The CC-8 is a communications processor that can serve as a plug-compatible front end to one or more 360-, 370-, or 303X-type computers. It has more features and is less expensive than the 3705 controller that it emulates, according to its manufacturer, Computer Communications Inc.

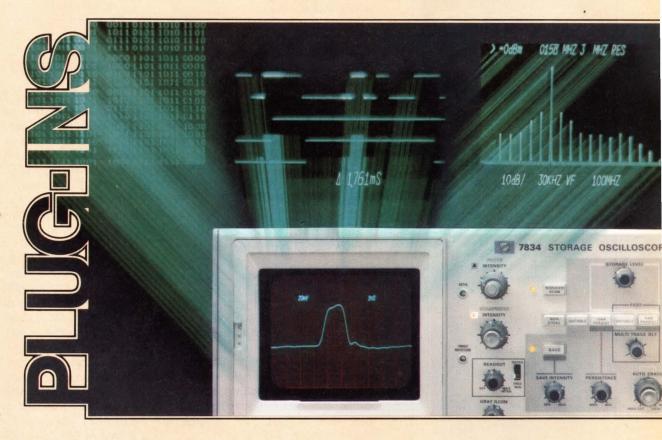
The system comes with a cathoderay-tube terminal that displays readouts of system line status, alarms, and statistical data in four colors when the CC-8 is used as a system monitor. In this mode, users can adjust over 60 types of errors.

The CC-8 also operates as a





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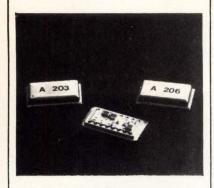
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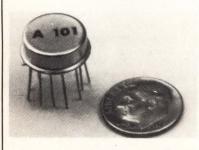
NEW PRODUCT

CHARGE SENSITIVE PREAMPLIFIERS



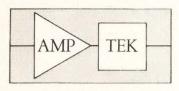
Models A-203 and A-206 are a Charge Sensitive Preamplifier/Pulse Shaper and a matching Voltage Amplifier/Discriminator developed especially for instrumentation employing solid state detectors, proportional counters, photomultipliers, channel electron mutipliers or any charge producing detectors in the pulse height analysis or pulse counting mode of operation.

These hybrid integrated circuits feature single supply voltage, low power dissipation (16mW), low noise, pole zero cancellation, unipolar and bipolar outputs and adjustable discrimination level.



Model A-101 is a Charge Sensitive Preamplifier-Discriminator and Pulse Shaper developed especially for instrumentation employing photomultipliers, channel electron multipliers and other charge producing detectors in the pulse counting mode. Its small size (TO-8 package) allows mounting close to the collector of the multiplier. Power is typically 15 milliwatts and output interfaces directly with C-MOS and TTL logic. Input threshold and output pulse width are externally adjustable.

All Amptek, Inc., products have a one year warranty.



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New products

system supervisor, permitting dynamic system reconfiguration and extensive control, including real-time assignment of lines and terminals within the network.

Designed for heavy communications traffic, it can handle a sustained synchronous throughput of over 200,000 characters/s and peak loads approaching 400,000 c/s. Furthermore, it supports most popular line disciplines and remote terminals, works with any mixture of line types and communications rates, and can control up to 240 lines.

Computer Communications Inc., 2610 Columbia St., Torrance, Calif. 90503. Phone (213) 320-9101 [366]

Space-saving printer saves capital too

In building desk-top computer systems, how much space and money does a designer want to devote to a printer? Integral Data Systems figures that the answer to both questions is: as little as possible. So it put together a tractor-fed impact printer called the Paper Tiger that has a paw-print of just 1.37 ft² and a single-quantity price of \$995.

The 121/4-in.-high printer doesn't skimp on features to realize its price. On fanfold or roll paper 1.75 to 9.5 in. wide, the unidirectional unit prints a 96-character ASCII set using a seven-by-seven-dot matrix. Character width is software-adjustable, so users can combine pitches of 8.3, 10, 12, and 16.5 characters/in. on a single line. With a single pitch, lines can be 73, 80, 96, or 134 characters long. Depending on pitch, they are printed at rates of 100, 120, 144, or 198 characters per second.

Switches set the line spacing at six or eight lines/in. and the form length from 3 to 14 in. An automatic 1-in. skip between pages is also selectable. For generating forms and other graphics, users can choose an optional package that provides both full dot-pattern control and a 2-kilobyte buffer that will store an entire 80-by-24-character page, the typical display capability of most low-cost

cathode-ray terminals.

Integral Data Systems, 14 Tech Circle, Natick, Mass. 01760. Phone (617) 237-7610 [365]

Midi mainframes distribute processing

To extend its so-called Distributed Systems environment into medium-scale mainframe computers, Honey-well Information Systems has introduced four new models. By so doing, the company is joining Burroughs and NCR [Electronics, March 15, p. 46] in responding to IBM's new low-end mainframe, the 4300 [Electronics, Feb. 15, p. 85].

There are two Level 64/Distributed Processing Systems, or DPSs for short. The DPS-320 can have from 512 kilobytes to 1 megabyte of main memory, five times the main memory capacity of the bottom-line Level 64 computers, and offers 50% more performance than those machines. The DPS-350, which can have up to 2 megabytes of memory, has 2.6 times the internal performance of the basic Level 64 and also 5 times the memory capacity. The DPS-320 is priced at \$81,360, 12% below the previous Level 64 computers, while the DPS-350, is priced at \$155,232, about 60% more than the current models. The former is scheduled for delivery in this quarter, the latter for the third quarter. Honeywell positions these units against IBM's 4331

Two other models add to the Level 66 offerings and compete with the IBM 4341. The DPS-440 offers twice the performance of the previous entry-level model 66/05 computer and sells for \$198,338 with 1 megabyte of memory or for \$265,397 with 2 megabytes. The even more powerful DPS-520 sells for \$371,316 with 1 megabyte of main memory, \$416,066 with 2 megabytes, and \$466,831 with 4. Deliveries of these two models are scheduled for early 1980.

Honeywell Inc., United States Information Systems Group, 200 Smith Street, Waltham, Mass. 02154. Phone (617) 890-8400 [363]



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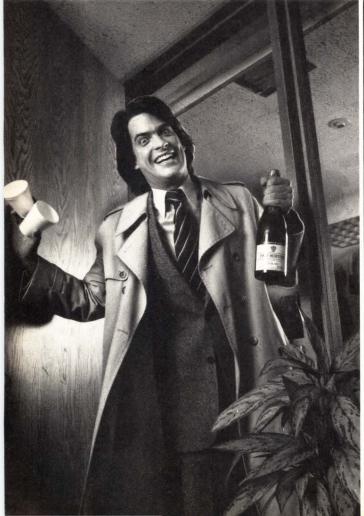


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Data acquisition

System acquires data, not space

Designed for the LSI-11/23 data-acquisition system can stand alone or work in net

Sometimes it is not the uniqueness of what you put in a package but the package itself that will make people sit up and take note. ADAC Corp.'s newest data-acquisition and control system, the System 2000, measures only 7 by $8\frac{7}{16}$ by $21\frac{1}{2}$ in.

Designed with Digital Equipment Corp.'s latest microcomputer in mind—the LSI-11/23 [Electronics, March 1, p. 34]—the System 2000 will house up to 13 half-quad (8.5-by-5-in.) boards. With them, it can act as a stand-alone control system or as a remote data station in a distributed processing network (with either an LSI-11/2 or LSI-11/23 on board). All LSI-11/2-compatible

analog and digital input/output systems from ADAC can also be used with the system.

"A lot of people don't need a large backplane; look at the size of the LSI-11/23 and its memory management chip," observes A. L. Grant, vice president of marketing and sales, "and the power supply in our System 2000 can support 128 kilobytes of memory." According to Grant, many earlier systems based on the LSI-11 and 11/2 could not begin to support that much memory with a single power supply.

The System 2000 has a transformer, which allows the system to be used anywhere in the world, and a dual power supply built into the back of the unit. The power supply operates at +5 v at 15 A, and +12 v at 3 A. The ±15 v needed for analog I/O boards is supplied by on-board dc-dc converters or a plug-in power supply board.

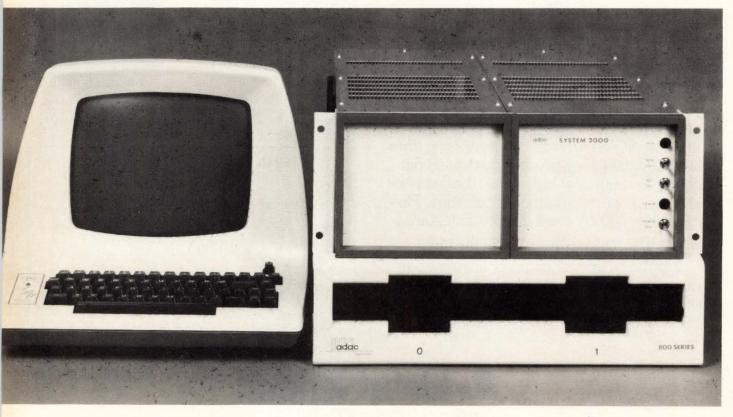
The front panel of the unit pulls off—it is secured by four spring clip fasteners—to allow easy access for any one of 13 cards; they slide in on two vertical tracks from the front. Inside the unit is a half-rack enclo-

sure, a 13-slot backplane and card cage, and the power supply. All I/O cables are routed to the right side of the card cage and through a slot in the back panel. There is a fan in the back panel to cool both the card cage and power supply.

If the user needs more than one unit for additional 1/O boards, a second System 2000—minus the front panel switches—with its own power supply can be purchased. Putting a bus-repeater card from ADAC in the first unit and cabling it to the second will complete the expansion.

A System 2000 with CPU and 32 kilobytes of memory, a CRT, serial port, and a double-density floppy-disk drive and controller, added to DEC software, will cost under \$10,000, according to Grant. "The hardware is also there for a development system for the LSI-11/23," he notes, although that's not being pushed until the LSI-11/23 is readily available in June.

Grant expects the System 2000 to complement and expand on ADAC's earlier System 1000. "It's also going to be used in process-control applica-





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single-beam or dual-beam models (the latter come in single- or double necked makes), rearwall-screen and on-screen-grid models. Vibro-shock-explosion-proof ELMITRONS can be safely used at high altitudes.



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New products



tions, as well as other industrial and scientific environments," he notes. "It can be put into dust-free enclosures—the size of the unit lends itself to those types of applications."

The system weighs about 25 lbs. The unit with power supply and card cage sells for \$995 in quantities of one to four. Shipments will begin in May, with deliveries 30 to 45 days after receipt of order.

ADAC Corp., 70 Tower Office Park, Woburn, Mass., 01801. Phone Al Grant at (617) 935-6668 [381]

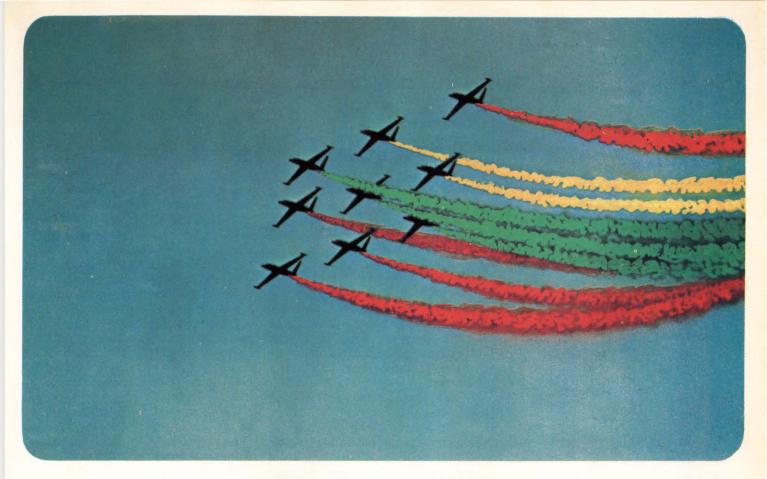
Board expands microNOVA analog input capacity

The ST-MNOVA-ADX series of peripheral slave expander boards for Data General's microNOVA microcomputers allows system expansion, in increments of 64 single-ended or 32 differential channels, up to 256 channels, when used with Datel's ST-MNOVA analog input/output master boards. The slave expander cards slide into and interface directly with the microNOVA bus.

Two ST-MNOVA-ADX boards are available: the 64-channel, single-ended ADX64S; and the 32-channel, differential ADX32D. Both feature a multiplexer crosstalk specification of 0.01% from dc to 1 kHz, both are powered by the master board, and both operate from 0° to 70°C.

Use of the differential-input board requires that the master board be fitted with an amplifier.

Datel Systems Inc., 11 Cabot Blvd., Mansfield, Mass. 02048 [383]



Fly by color!

The Electron Tube Division is now readying a range of specially ruggedized, extremely high brightness, high-resolution, multicolor CRT's, destined for the head-down display (HDD) systems of the new generations of civilian and military aircraft that are being developed for the 1980's. The use of these tubes in HDD's permits displaying several different parameters simultaneously on a single screen, by using different combinations of scanning standard (TV or stroke-writing) and color. This reduces total display area, simplifies data assimilation, and reduces recognition errors. All of these new tubes will use the penetration screen principle. pioneered by THOMSON-CSF. Typical of

these new tubes is a 5" x 5", 3-color, high-resolution tube with a contrast-enhancing directional filter. Primarily destined for the MIRAGE 2000. the new French combat aircraft, this tube, or a derivative thereof, is suitable for any military aircraft in which high readability is required under the intense lighting commonly found in cockpits. Similar tubes have been developed for civilian aircraft where environmental conditions are slightly less severe. In addition, because the copilot must have access to the same information as the pilot, these tubes use wide-viewing-angle, neutral-density filters for contrast enhancement, instead of directional filters.







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New products

Communications

Optic modules are affordable

Transmitter and receiver link TTL-level devices for as little as \$49.95 each

Like any new technology, communication through fiber optics will gain public acceptance when functionally complete and affordable units are available. Fitting that bill are a compact transmitter and receiver from Spectronics Inc., a Honeywell subsidiary.

The company, long known in the military market for highly reliable optical products, is launching a full fiber-optic family of parts for commercial applications. The SPX 4140 transmitter and SPX 4141 receiver optically couple transistor-transistor-logic-level signals through a variety

of single-fiber cables, including plastic or glass strands from Siecor, Galite, and Dupont. The modules incorporate integrated-circuit chips in leadless carriers to control interfacing functions. Either one sells for \$49.95 in quantities of 1,000.

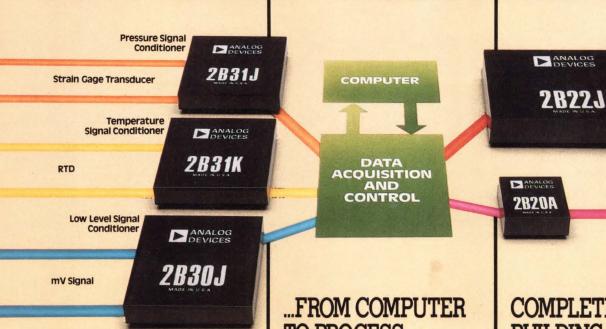
The transmitter IC (SPX 3619) has a high-speed current driver that works in conjunction with an 820-nm light-emitting diode. The companion IC (SPX 3620) for the receiver transforms low-level signals from a p-i-n or avalanche photodiode into a TTL output. The link will transfer Manchester-encoded data at rates up to 10 megabits/s over distances up to 2 km with no need for external fine-tuning. It will operate in the 0°-to-70°C range.

Transition and propagation times of the transmitter's LED are 7 and 5 ns, respectively. It exhibits peak output at a current of 150 mA.

The photodiode, a transimpedance preamplifier with automatic gain control, and a post-amplifier comparator and buffer comprise the receiver. Its sensitivity for Manches-



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The 2B22 offers 4 to 20mA output with ±1500V dc input to output isolation to eliminate ground loops and to protect against high voltage transients. It meets IEEE Std 472 for transient protection (SWC). \$59 in 100's (2B22J).

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For complete information, call Janusz Kobel at 617/329-4700. Or, write Analog Devices, Inc., P.O. Box 280, Norwood, MA 02062.



WAYOUT IN FRONT.



Now Gould offers a range of digital storage oscilloscopes that offer a world of advantages over conventional tube storage technology, beginning with being able to capture transient or "one-time" events and

store them indefinitely for display or hardcopy printout. This makes them ideal for electronic, electromechanical, educational, and biophysical applications.

Both the OS4000 and the new OS4100 combine the capabilities of semi-conductor memory with a bright, stable,

flicker-free display. This technique allows analysis of signal build-up and decay characteristics through pre- and post-trigger viewing. Expansion of the display after storage permits detailed study of specific areas of the trace.

The new model—OS4100—also offers you stored X-Y displays, channel sum or

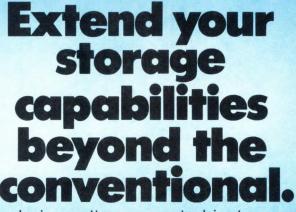
difference and a maximum of 100μ V per cm sensitivity with noise suppression. A unique trigger window circuit assures capture of transients of unknown polarity.

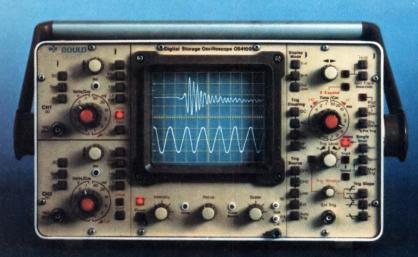
Other outstanding features include

automatic operation, display of stored and real time traces simultaously and hard copy memory output in digital or analog form. And IEEE488 is available for compatible interfacing.

If features like these aren't enough to lure you away from less sophisti-

cated instruments, remember that Gould scopes are backed by a two-year warranty of parts and labor, exclusive of fuses, minor maintenance and calibration. And application assistance, customer training and worldwide service centers are part of Gould's customer support program.





Gould manufactures 60% of the world's digital storage oscilloscopes.

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For detailed information or an on-site demonstration of any oscilloscope in the Gould line, contact Gould Inc., Instruments Division, 3631 Perkins Avenue, Cleveland, OH 44114. In Europe contact Gould Instruments, Roebuck Road, Hainault, Essex England 1G6 3UE.

For brochure or demonstration call toll free (800) 325-6400, Ext. 77. In Missouri (800) 342-6600, Ext. 77.



New products

ter-encoded data is 200 nA at 10 Mb/s, with a 10⁻⁸ bit error rate.

Both modules work off a single +5-V supply and they can be easily connected to optical SMA-style connectors. Standard versions are equipped with Amphenol fiber-optic connectors but other connectors can also be provided.

The exit aperture of the LED is guaranteed to be 300 μ m and typical output power is 0.7 mW. This is achieved by using a reflective cone that in effect places the emitter chip directly in contact with the flat window of the LED package while enlarging the target area. The approach permits high-volume production and also yields a low price. Spectronics Inc., 830 East Arapaho Rd., Richardson, Texas 75081. Phone (214) 234-4271 [401]

Lightweight TWTA delivers 5.5 W

Originally developed for the Tracking and Data Relay Satellite (TDRS) system, the model 1264H is a traveling-wave-tube amplifier that delivers 5.5 W in the 3.7-to-4.2-GHz range.

The unit is based on the model 230H TWT and was designed for high efficiency, ruggedness, and light weight. It has a saturated gain of 55 dB, an expected operating life of 10 years, and weighs 3 lb.

Hughes Electron Dynamics Divison, 3100 West Lomita Blvd., Torrance, Calif. 90509. Phone (213) 534-2121 [403]

Receiver meets changing needs by changing modules

The model SR-2093 is a vhf-uhf surveillance receiving system that uses a synthesized local oscillator. Designed to accept a variety of modules, it can be changed to fulfill different tracking requirements.

The system can be tuned from 20 to 500 MHz and provides a choice of three intermediate frequencies: 20 kHz, 300 kHz, and 4 MHz. The range can be expanded to 1,200 MHz

and additional intermediate frequencies can be selected. Memory, single-sideband detectors, and other options may also be specified.

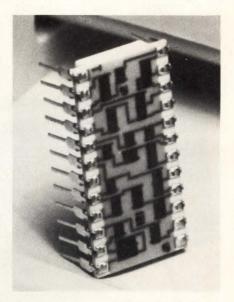
The receiver may be operated locally or remotely and features a liquid-crystal display of all tuning information.

Norlin Communications Inc., 9125 Gaither Rd., Gaithersburg, Md. 20760. Phone Don Biscoe at (301) 948-5210 [408]

Chip set filters DTMF signals

Designers digitizing telephones can now turn to two 24-pin devices to do their dual-tone-multifrequency (DTMF) filtering. One, the AF121, separates the 697-to-941-Hz frequencies while the other, the AF122, tackles the 1,209-to-1,633-Hz zone.

Used together, the sixth-order elliptic filters provide 40 dB group separation as well as 40-dB separation from the dial-tone frequency. They can be purchased with a maximum peak-to-peak ripple of 2 or 4 dB in the passband and are priced



accordingly at \$27.50 and \$24.50 in small quantities. Delivery time is three weeks.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone Dennis Dauenhauer at (408) 737-5848 [409]

Instruments

Smart counters cost little

120-MHz and 1-GHz units make measurements quickly and automatically

One measure of the "intelligence" of a so-called "smart" instrument is the complexity of its front panel. A really smart machine should have a fairly simple set of controls, since it requires little user intervention. By this criterion, two new microprocessor-based frequency counters from Philips belong near the top of the class. Aside from their seven-digit displays and input connectors, all these counters have on their front panels are an on/off switch, a sensitivity control, and a two-position measurement-rate switch.

A patented automatic trigger level circuit gives the 120-MHz PM 6667 and the 1-GHz PM 6668 the capability of triggering reliably on a wide variety of waveforms, including pulse trains with low duty cycles.

The counters make high-resolution measurements of low frequencies by taking multiple period measurements and computing the reciprocal value. The microprocessor eliminates the need for long gate times, gets rid of the usual ±1-Hz error, and overcomes the limitations of phaselocked frequency multipliers. This means that a tone frequency of, say, 988.1183 Hz or a line frequency of 60.81253 Hz can be measured to seven places in only one second. Furthermore, range setting, decimalpoint positioning, and indication of units (kHz, MHz, etc.) are all done automatically.

Cutting costs. In addition to providing brain power, the microprocessor helps to cut costs by eliminating many components. The designers of the counters really concentrated on this area by using monolithic front-end circuits and by making extensive use of large-scale integration in the logic circuitry. The result is that the 120-MHz counter sells for only \$425 and the 1-GHz instrument goes for \$545. Included in the higher-frequency counter is an automatic p-i-n diode attenuator that provides protection against signal levels that might do damage to the sensitive input circuitry.

The measurement-rate switch gives users a choice of two measurement times: 1 s and 200 ms. The normal (1-s) time yields the full frequency resolution of seven digits. The fast speed makes it easier to track changing frequencies—when making adjustments, for example—but trades off resolution, reducing it to six digits.

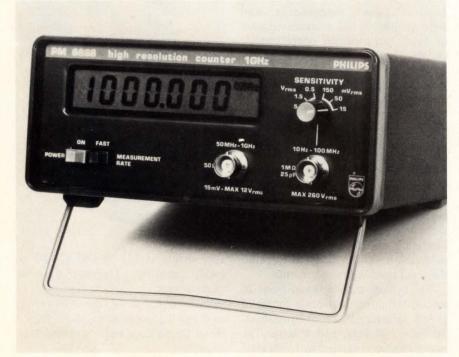
The six-step attenuator, which allows the sensitivity to be adjusted from 5 V rms down to 15 mV rms, is claimed to provide up to 10 dB more noise immunity than conventional ×10 attenuators. When it is in its most sensitive position, the input sensivity of the high-impedance input is 15 mV rms for sine waves from 10 Hz to 75 MHz and 25 mV rms for sine waves from 75 MHz to 120 MHz. For pulses with a duration of 7 ns or more, the sensitivity is specified at 45 mV peak to peak.

In addition to the high-impedance (1 M Ω shunted by 25 pF) input, the PM 6668 has a 50- Ω input, which is not affected by the sensitivity control. This rf input has a sine wave sensitivity of 15 mV rms from 70 MHz to 500 MHz and 25 mV rms from 500 MHz to 1 GHz.

Both meters can be supplied with an optional battery pack that provides up to five hours of uninterrupted operation. The use of a liquid-crystal display allows a large readout (11.5-mm digit height) with little effect on battery life.

Built around crystal oscillators that drift less than one part in 10⁷ per month, the new counters are given a comprehensive check-out every time they are turned on. If they fail the test, a diagnostic code appears on the display.

Philips Test and Measuring Instruments Inc., 85 McKee Dr., Mahwah, N. J. 07430. Phone (201) 529-3800 [351]



4¹/₂-digit true-rms multimeter sells for \$345

The model 4020 digital multimeter is a 4½-digit instrument that can resolve voltage to 10 μ V, current to 10 nA, and resistance to 10 m Ω . Its

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New products



basic measurement uncertainty, in the dc-voltage mode, is $\pm (0.02\%)$ of reading + 1 count). The unit measures ac and dc voltage, ac and dc current, and resistance. The ac ranges respond to the root-mean-square value of the input signal.

Overload-protection circuitry allows all of the dc-voltage ranges to withstand up to $\pm 1,200$ V, all of the ac-voltage ranges to take up to 500 V rms, and all of the resistance ranges to survive up to ± 250 V dc or 250 V rms. All current-measuring ranges are protected up to 2 A; the 10-A range up to 15 A.

The basic DMM 4020 lists at \$345. The 4020 B, which includes nickel-cadmium batteries, is priced at \$360. A version with binary-coded-decimal outputs, the 4020 C, goes for \$445. And the model 4020 BC combines batteries and BCD outputs for \$460.

Kontron Electronic Inc., 700 South Claremont St., San Mateo, Calif. 94402 [353]

Plug-in pulse driver puts out ± 15 V at 30 MHz

Designed to plug into Tektronix TM-500 series power modules, the model PI-454 pulse driver is a 30-MHz instrument that can deliver ± 15 v across 50 Ω . Intended for driving second-generation chargecoupled devices and complementarymetal-oxide-semiconductor circuits, the driver accepts transistor-transistor-logic levels and boosts them to the desired output level. The high and low output voltages are independently adjustable by means of a front-panel control. They may also be voltage controlled or (optionally) digitally programmed. In unit quantity, the PI-454 sells for \$475.

Pulse Instruments, 1536 West 25th St., San Pedro, Calif. 90732. Phone Dave Kan at (213) 541-3204 or 548-1327 [356]

Once you compare our new 191 digital multimeter to ordinary 5½-digit DMMs, we think you'll readily agree that it outclasses its class. For good reason.

The 191 is a $\pm 200,000$ -count DMM capable of 0.004% accuracy and $1\mu V/1m\Omega$ sensitivity. It delivers unsurpassed accuracy, faster, because firmware in the 6802-based accuracy, faster, because firmware in the 6802-based accuracy faster, because firmware in the 6802-based accuracy.

precise analog circuitry.

Displayed data is updated at the fastest rate of digit change readable by the human eye—4 conversions per second. Settling time of 0.5 seconds is easily half that of the 191's nearest competitor.

The µP combines both charge-balance and single-slope conversion techniques. Every displayed reading is automatically corrected for zero and gain drift.

If you've ever had to contend with the frustration of potentiometer zeroing, you'll appreciate the 191's null function. Automatic arithmetical correction of residual error is standard. With a touch of the button you can buck out any in-range signal, large or small.

Ayear from You don't need low-level noise either. So the 191 automatically suppresses it. The 191's non-linear digital filter is entirely free of dielectric absorption and leakage problems associately with analog techniques. On the 200mV and 200Ω ranges, the filter effectively attenuates noise by displaying a running average of the You don't need low-level noise either. So the 191 autoentirely free of dielectric absorption and leakage problems associated with analog techniques. On the 200 mV and 200Ω ranges, the filter effectively attenuates noise by displaying a running average of the

8 previous readings. Yet it instantly displays input changes of 10 digits or more.

own one or wish

Another exclusive of the 191 is 2 and 4-terminal measurement from $1m\Omega$ to $20M\Omega$ across six ranges. Simply adding two more sense leads automatically enables Kelvin measurements. No changing input terminal links or even pushbutton settings.

And, finally, since µP design reduces component count, the 191 requires less servicing and calibration,

increasing reliability and stability.

At \$499 without plug-in ACV, the 191 is today's performance/value leader in 5½-digit DMMs. A year from now most people will agree.

But you probably don't need that much time to make up your mind. And we're ready to help you with a demonstration or additional information. Call 800-321-0560. In Ohio, 216-248-0400.

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Modular printer marks parts fast

Components of all types are handled by versatile print-and-cure system

"Increased efficiency and flexibility are the two main thrusts of the manufacturing environment of the 1980s," says Bill Lynch, product manager for electronics and electrical industries of Markem Corp., Keene, N. H. To meet these trends, Markem has produced a fully automated modular component printing system called the series 3000. Components in lead frames or unattached parts can be handled by the new printer. In addition, depending on the type of part, one operator using the new printing system can churn out printed parts at rates varying from 5,400 to 21,600 units per hour.

Flexibility of the series 3000 is obtained by breaking the system down into a series of functional modules. These are composed of a single print module, two partsconveying modules, three partshandling modules, and three curing modules. The modules are assembled to suit the type of component to be marked.

Key modules of the series 3000 are the two parts-conveying mod-

ules: one for attached parts such as dual or single in-line packages in lead frames and capacitors in strips, the other for separate parts such as switches, relay housings, cases, TO-3s, or DIPs in sticks.

The conveyor in the photo is for attached parts. It is a microprocessor-controlled unit that features low-cost, quick-change belts and product guides, which assure that parts are properly presented to the print station for accurate registration. Each belt is "programmed" with eyeholes that activate photocell controls in the print module. Changing the belt and guide for one product to those for another requires no more than five minutes.

Cycle rate for attached parts ranges from 7,800 to 21,600 per hour, depending on operator skill and parts configuration. This is five times as fast as older Markem printline systems.

The unattached-parts conveyor offers a variable cycle rate up to 5,400 components per hour, depending on size, parts configuration, and operator skill.

Parts-handling modules are available to help increase throughput for several major applications. For instance, products in strips may be hand-fed more smoothly and efficiently with a specially designed feed assist. Alternately, lead-frame magazine loaders and unloaders, engineered at the factory to the user's specifications, allow a cycle rate of 13,000 parts per hour with real throughput up to 80%; and stick

unloading and reloading mechanisms for 300-, 400-, 600-, and 900-mil DIPs provide a cycle rate of up to 11,000 per hour, also with high real throughput.

A refined design of Markem's highly reliable rotary offset print module does the actual printing on the series 3000. The offset wheel is retractable, providing registration capability for products in strips on close centers.

The dual tangicam typeholder accepts all commonly used printing elements, including rubber plates, Markem type, and plates made in the user's plant with the Markem model 452 Platemaker System.

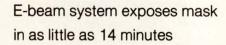
Integral curing modules of three types—ultraviolet, serpentine, and infrared—will be offered to help component manufacturers increase the productivity of their mark-and-pack operations. In-line print curing reduces the amount of product handling required and frees floor space that would otherwise be needed for a batch curing oven.

Ultraviolet curing, available immediately, provides a quick cure with low heat to substrate and low energy consumption. Infrared and serpentine curing modules for the series 3000 are under development.

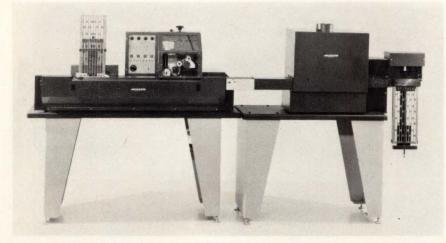
Price for a print-cure system with the attached-parts conveyor is between \$40,000 and \$45,000, whereas the cost of a system built around the unattached-parts module is in the region of \$25,000.

Approximate dimensions of the series 3000 are 4 feet high by 10 feet wide by 2 feet deep. Approximate weight is 1,400 lb.

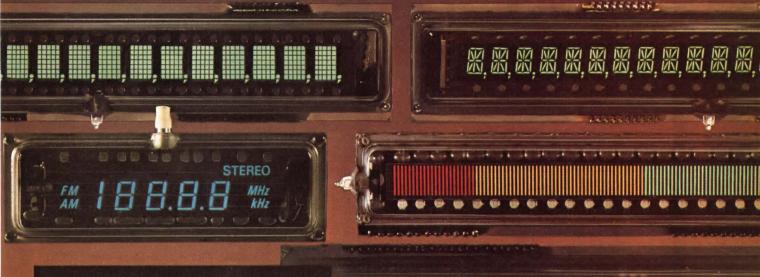
Markem Corp., 150 Congress St., Keene, N. H. 03431. Phone (603) 352-1130 [391]



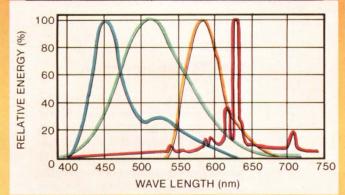
An electron-beam lithography system can etch circuit patterns with lines and spacings as fine as 1 μ m, so that as many as 15,000 circuits can be fabricated on a 4-inch silicon wafer. Using a 0.5- μ m address structure, the Ee-BES 40 can expose an



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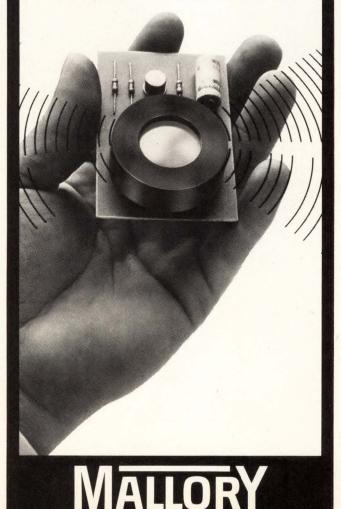
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overseas. Give us a hearing. Write or call. P. R. Mallory & Co. Inc., Box 1284, Indianapolis, Indiana 46206. (317) 856-3731.





New products



area of 5 cm² per minute so that a mask for a 4-in. wafer can be exposed in as little as 14 minutes.

The mask cassette handling system of the unit operates without interruption for 8 hours. To start production, a magazine is manually loaded with up to 10 cassettes that each hold the parameters of a single mask. The magazine is then loaded into the vacuum system by a four-position elevator. The magazine remains under high vacuum in an antechamber while the handling system automatically transfers cassettes to and from the writing chamber.

The machine has a throughput rate of 40 MHz, which is twice as fast as other mask-making machines, according to the company. The work chamber accommodates 6-in. masks. The Ee-BES 40 sells for about \$1.7 million and delivery is scheduled for the fall of 1979.

Varian/Extrion Division, Blackburn Industrial Park, Gloucester, Mass. 09130. Phone (617) 281-2000 [394]

Machine terminates 2- to 24-wire assemblies

The CT-1347 harness-fabrication machine can simultaneously terminate discrete wire assemblies having from 2 to 24 wires at a rate of 500 per hour. The wires may vary in length from 8 to 50 in. Lead lengths may be changed in the machine, and the wires can be terminated by stripping them or with a Jaguar connector. The machine sells for \$25,000. Delivery takes 10 to 12 weeks.

Methode Electronics Inc., Interconnect Products Division, 170 Hicks Rd., Rolling Meadows, Ill. 60008. Phone (312) 392-3500 [396]





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Pascal resides in PROM

UCSD Pascal firmware for 6800 and 6809 processors eliminates interpreter software

Getting Pascal up and executing on a microprocessor is easier said than run. One hurdle has been that the widely attractive UCSD versions of the language require interpreters to reside on target machines. While an interpreter can be written in software, the process takes time and money. So Control Systems Inc., Kansas City, Kan., is now offering a series of programmable read-only memories with interpreters for various versions built in.

CSI put a pseudocode (or p-code) interpreter for UCSD Pascal in ROM for use with its UDS 470 development system [Electronics, Dec. 21, 1978, p. 128]. "The response to that product convinced us to sell the interpreter separately," says Dave Allen, technical manager of CSI's Microsystems division.

Firmware is currently being supplied for the 6800 and 6809 microprocessors, and other interpreters for the 16-bit 68000 are being considered. Various interpreter versions work with the different versions of UCSD Pascal, providing such capabilities as execution of floating-point operations.

Prices for Pascal in PROM range from \$145 for a 6800 interpreter (version II.O UCSD Pascal with floating-point math) to \$210 for a 6809 interpreter (version III.O with floating-point capability). Code is supplied in 2716 erasable PROMS; special arrangements can be made for interpreters stored in other memories, as well as for ones that work with development systems other than the UDS 470.

Control Systems Inc., 1317 Central, Kansas City, Kan. 66102. Phone Kathleen S. Micken at (804) 564-9350 [371]

Cross assembler for 8086 is priced at \$80.86

Although users have been able to buy Intel's 8086 microprocessor for over a year now [Electronics, Feb. 16, 1978, p. 99], the company just recently unveiled the much-needed hardware and software support [Electronics, March 1, 1979, p. 184]. Although additional support is expected from outside sources like universal development system manufacturers, would-be 8086 users are becoming increasingly frustrated with the delay. But a small company in Medfield, Mass., has a software package that will not only alleviate frustration, but also lower costs and programming time.

The company is Security Research Laboratories Inc. and the software package is a cross assembler that will run on any computer with file-structure Basic. "The software available with Intel's 8086 development system is intended for management people," notes Victor A. Bennett, director of research and development. "It's not for software programmers." But SRL's cross assembler is "written by programmers for programmers," according to Bennett, and as such, has many extras to ease the programming burden.

All the user needs is a computer that supports Basic, with a file structure and at least 16 kilobytes of memory; if there's more memory, the program will run faster. Either interactive or compiled Basic can be used; however, the cross assembler does use Dartmouth's standard for floating-point math. "The cross assembler produces code in the same format as the 8086," says Bennett. The object code produced is 8086 machine language.

The entire cross assembler runs to about 1,000 lines, and with the efficiency of the mnemonics, the programmer can save about 60 to 70% in typing time, Bennett says. "With a PDP-11/34, the cross assembler runs at about 1,000 lines per minute," he comments. He estimates

Divide and Conquer

a full program might take one to four minutes, depending on the type of machine used and the length of the program. Another nice feature: SRL's cross assembler prints a listing of errors as they occur.

So, instead of spending up to \$20,000 on a full-blown development system, the user can buy a cross assembler from SRL for \$80.86 to run on his own machine providing, of course, that he has one. For this price he gets a source-code listing, an instruction manual containing all the operating instructions for the software, and the mnemonics for the 8086 microprocessor. Also included is a condensed version of the instruction manual for easy referencing. SRL plans to offer the program on floppy disks and tapes shortly.

Delivery time is three weeks.
Security Research Laboratories Inc., P. O.
Box 49, Medfield, Mass. 02052. Phone Bob
Smith at (617) 359-6950 [372]

DMA controller for TMS 9900 offers fast I/O at low price

With redoubled attention to its TMS 9900 line, Texas Instruments is offering a direct-memory-access (DMA) controller it claims will make high-speed input and output practical at very low cost.

Designated the TMS 9911, the chip generates memory-control signals and sequential memory addresses for two separate channels. It does so without relying on an external device such as a central processing unit. Thus, it provides I/O independently, at rates of one million 16-bit words/s. The 40-pin unit sells for a price of \$15.40 in quantities of 100 or more.

For access, the unit takes control of a system's memory bus, shutting out the CPU and other DMA controllers. (Multiple TMS 9911s may be used if more than two DMA channels are needed.) After each byte or word access, the address is automatically incremented and compared to a value stored in a last address register. A status bit and CPU interrupt are generated when the values coin-

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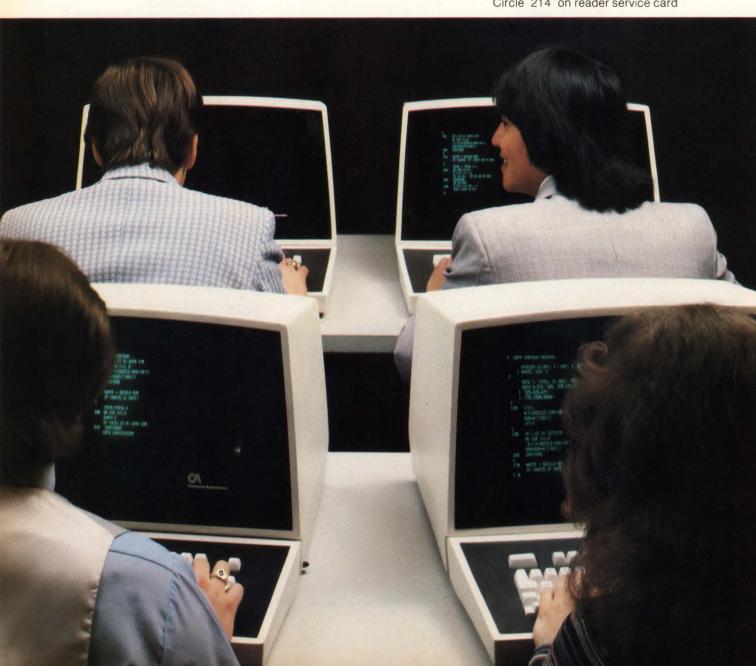
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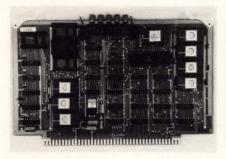
New products

cide, indicating transfer completion.
Texas Instruments Inc., Inquiry Answering
Service, P. O. Box 1443, MS-6404 (Attn:
TMS9911), Houston, Texas 77001 [374]

Package paves way for forthcoming MC6805

An MC6805 simulator module, a floppy disk with a linking loader, a demonstration program, a cross assembler for macrocode, and an instruction manual comprise the MEX6805SIM. With this package, system designers and programmers can familiarize themselves with the MC6805 single-chip computer that will very shortly become available from Motorola.

The package simulates the computer's entire instruction set and interrupt-driven routines, with provision for user reset and timer interrupt signals. It features full trace capability and traps all invalid instructions, effective addresses, stack pointer overflows and underflows, and program counter over-



flows. Nonmicroprocessor features of the MC6805 can be emulated using an MEX68USM universal support module configured in accordance with instructions in the supplied manual.

The simulator module plugs into an EXORciser 1 or 1A or an EXORterm 200. Minimum system requirements also include an EXORdisk II, an editor, and 24 kilobytes of memory, as well as a terminal. The MEX6805SIM package is priced at \$2,500.

Motorola Microsystems, P. O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 962-2223 [378]

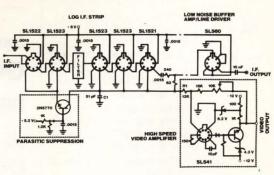
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The SL541 lets you vary video sensitivity, and has the high slew rate (175 V/ μ sec), fast settling time (1% in 50 ns) and high gain stability you need, with on-chip compensation so it's not tricky to use.



The SL560 on the IF output is a "gain block" that replaces your hybrid and discrete amplifiers, usually with no external compensation. Noise figure is under 2 dB, gain up to 40 dB, and the bandwidth is in excess of 320 MHz.

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New products

Semiconductors

Generator drives bar-graph displays

Aimed at audio applications, IC works with both LED and vacuum-fluorescent displays

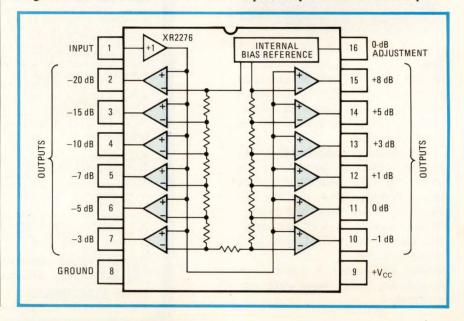
There is a growing trend in the design of audio equipment, both professional and consumer, to replace conventional volume-level (VU) meters with bar-graph displays, which respond better to instantaneous peaks. Designers are looking for easy ways to make the swap, and Exar Integrated Systems Inc. feels it has an answer in its XR-2276 bargraph generator circuit.

Similar in design to National Semiconductor Corp.'s LM3914 [Electronics, July 20, 1978, p. 161], the monolithic device is distinguished by several characteristics that reflect particular requirements and preferences in the audio market, according to Exar's vice president of engineering and marketing, Alan B. Grebene. "Instead of 10 bar-graph elements, the 2276 drives up to 12 and will drive vacuum-fluorescent displays, too," he points out, referring to the fact that the LM3914 drives light-emitting-diodes only.

Audiophiles prefer a 12-point bar graph to the 10-point type and find fluorescent displays more pleasing to look at, Grebene claims on the basis of information he has gathered from makers of audio equipment. He estimates the market for this \$2 chip (in quantities of 100 and more) to be greater than 200,000 devices, not counting what the Japanese may see fit to buy. "Japan," he acknowledges, "is where the big volume is, but we have a few key U.S. manufacturers who make high-priced audio systems, and they are looking for 50,000 to 100,000 parts each for the first year."

The 2276 is a relatively simple bipolar device, consisting of 12 voltage comparators whose inverting inputs are connected to taps along a resistive voltage-divider string, an input buffer amplifier whose output feeds the noninverting input of all of the comparators, and a 0-dB reference supply that may be programmed by means of a single external resistor. The reference supply provides the excitation voltage for the multitapped voltage divider; it therefore sets the 0-dB point for the meter-replacing display.

The chip's operation is straightforward. With no input signal, the comparators are all in a low-output state. As the input increases, it sequentially reaches each compara-



tor's inverting-input voltage, causing the comparator to turn on and drive the next bar-graph element. Best resolution is obtained around the 0-dB point, decreasing as the reference-voltage increments get larger toward the high (+8-dB) and low (-20-dB) ends.

With a supply voltage of 18 v dc and an ambient temperature of 25°C the 2276 will draw no more than 20 mA of current. The maximum current at the signal-input pin is 300 nA and the maximum input offset voltage is 1.6 v, both also at 25°C. The device will operate from 0° to 75°C.

Exar Integrated Systems Inc., 750 Palomar Ave., Sunnyvale, Calif. 94088. Phone (408) 732-7970 [411]

1-K static RAM is a power miser

Designers who must be stingy with power, such as those who make smart portable instruments, will want to investigate a 1-K static readwrite memory dubbed the MN5101. Fabricated using complementary-metal-oxide-semiconductor technology, the 256-by-4-bit random-access device consumes only 1 mW on standby.

The unit's chip is only 18 mm² in area—about 15% smaller than conventional C-MOS memories. It operates from a single +5-V power source and can access stored data in only 800 ns. The 22-pin RAM works with transistor-transistor-logic—level signals and has three output states for easy connection to microcomputer buses.



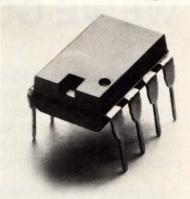
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Panasonic Corp., One Panasonic Way, Secaucus, N. J. 07094. Phone Bill Bottari at (201) 348-7276 [413]

Dual JFETs for scope input come as chips or in cans

Consisting of two junction field-effect transistors on a single chip, the SSD3578 and SLD3579 are intended for use as high-frequency front ends on oscilloscopes. In 100-piece lots, the TO-77-can version is priced at \$3.75 and the chip version at \$1.50.

The dual JFETs have a smallsignal common-source forward transfer admittance of 7.5 millimhos. Their gate-to-source leakage is less than 50 pA. Gate-to-gate leakage and parasitic capacitance are a low 50 pA and 3 pF, respectively. The noise figure is 3 dB.

The chip is constructed using V-groove technology to achieve junction isolation and has expanded contacts traversing the isolation moat, to increase reliability.

Texas Instruments Inc., Inquiry Answering Service, P. O. Box 225012, MS/34 (Att: SSD3578/SLD3579), Dallas, Texas 75265 [415]

Transceiver handles eight IEEE-488 bus lines

The MC3447 is a transceiver that conforms to the IEEE-488-1975 bus standard. Unlike other transceivers, which can handle only four of the bus's 66 lines, the MC3447 can work with eight.

The unit's low, 95-mA power consumption is achieved by allowing the seven noncritical channels to have a worst-case propagation delay of 50 ns. The eight, critical line has a worst-case propagation delay of 30 ns low to high or 22 ns high to low. In hundreds, the MC3447 costs \$3 in a plastic package, \$3.75 in ceramic. Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Ariz. 85036 [416]

And now, powerless memory

The addition of non-volatile memory to standard logic functions in Plessey's NOVOL series may be the most exciting news since the abacus.

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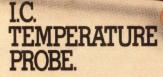
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DEC cuts cost of LSI-11/2 . . .

Digital Equipment Corp., Maynard, Mass., has lowered the price of its LSI-11/2 microcomputers by as much as 24%. Introduced in November 1977 [Electronics, Nov. 24, 1977, p. 50], the original LSI-11/2 with 64 kilobytes of working memory sold for \$2,490; it is now priced at \$1,900. For a unit with 32 kilobytes of memory, the price has been dropped from \$1,690 to \$1,490.

. . . and triples memory capacity of DECsystem 20

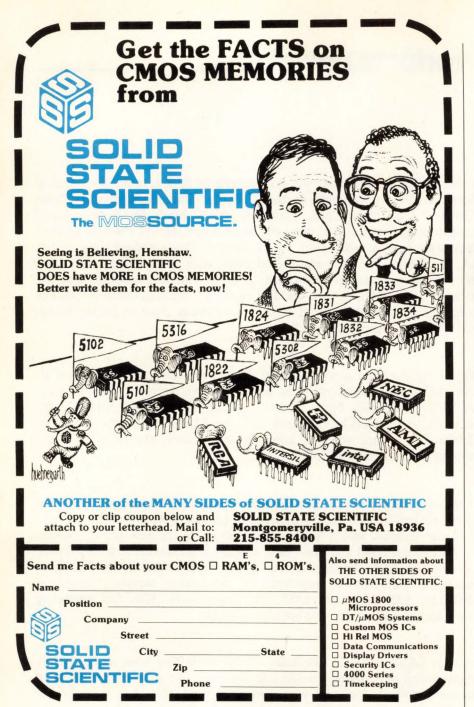
Three new DECsystem 20 mainframe computers use metal-oxide-semiconductor devices in their main memories to provide three times the capacity of earlier systems, which had magnetic cores. In the new configurations, the DECsystem 2040 and 2060 each support a maximum of 6 megabytes, whereas the 2020 supports 2 megabytes. Basic 2020, 2040, and 2060 packages, including 1 megabyte of solid-state memory, begin at \$161,000, \$359,600, and \$485,100, respectively. Kits for upgrading computers already in the field are also available.

Custom keyboards cost little, even in small quantity

Unicorn Engineering Co., Berkeley, Calif., is shifting from its first year's research and development mode into the manufacturing of small lots of custom keyboards for users who need only small quantities, according to founder Steve Gensler. The custom boards will be similar to an 11-by-21-in., 128-key product Unicorn developed for systems made for the physically handicapped. They use membrane switch technology, are environmentally sealed, and have adjustable sensitivity. Custom legends are easily inserted beneath the clear upper membrane. The large keyboards sell for \$75 each and the smaller ones will be proportionately less expensive. Prototype charges will vary from a minimum of \$200 to as high as \$900, according to Gensler.

Motorola packages triacs for consumer applications

Motorola Semiconductor Products Inc., Phoenix, Ariz., has put its 15-A to 40-A triacs, the MAC20/25/50, into a new package that makes them well suited for both consumer and industrial applications. The hermetic package, which has a base like that of a TO-3 can, has just received UL recognition. Its solderless terminals are expected to help cut costs in both appliance assembly and repair.



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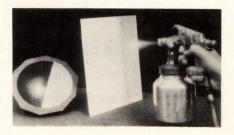


70,000 to 80,000 centipoises, a sheet resistivity of less than 0.04 ohm/square/mil, and a bulk resistivity of 2×10^{-5} ohm-cm. In lots of 50 grams, the material sells for \$1.25 per gram and in quantities of 1,000 g, 23 cents per gram. Delivery time is two to three weeks.

Aremco Products Inc., P. O. Box 429, Ossining, N. Y. 10562 [476]

A conductive resin coating, Eccocoat CC-30, is a one-component material that can be air-dried at room temperature in 15 to 30 min. It can be brushed or sprayed on, or the material to be coated can be dipped into it. Eccoat CC-30 has a surface resistivity of 1 Ω /sq and will not be affected when bent over a 0.25-in. (0.635-cm) mandrel. It will operate over the temperature range of '-65 to $+350^{\circ}$ F (-54 to $+177^{\circ}$ C). It has a shelf life of at least six months when stored in a sealed container at temperatures below 25°C.

Emerson & Cuming Inc., Dielectric Materials Division, Canton, Mass. 02021 [478]





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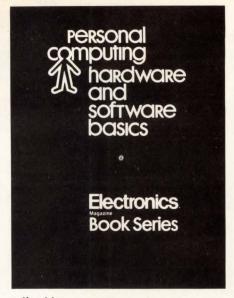
At your fingertips, all the most needed information on...

- what's available in personal computers
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- Electronics Datamation Mini-Micro Systems BYTE
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edited by Raymond P. Capece, Solid State Editor, Electronics Magazine 266 pages, \$11.95

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Part 1: Introduction to Personal Computing.
The term defined, equipment and components, costs, applications.

Part 2: **Basic Computer Theory.**Microcomputer architecture with the emphasis on memory.

Part 3: **Advanced Microcomputer Theory.**Board-level computers using the most popular microprocessor chips.

Part 4: **Reviews of Personal Computers.**Features and capabilities of the most widely used microcomputers.

Part 5: Software for Microcomputers and Microprocessors.

Description and uses of both machine-level and high-level programming languages.

Part 6: Specifications and Other Useful Information.

Glossaries, microprocessor specs, electronics symbols, buying used equipment.

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Maskmaking. A four-page brochure delineates the mask-making capabilities of Electromask Inc. and lists the specifications that the company can meet. Electromask Inc., E-Mask Division, a subsidiary of TRE Corp., 6109 De Soto Ave., Woodland Hills, Calif. 91367 [430]

Semiconductor equipment. Specifications and illustrations for more than 800 semiconductor processing and handling products are contained in Fluoroware's 1979 products catalog. Among these items are: injection-molded processing carriers, tanks, trays, tweezers, tongs, beakers, chip trays, and storage and shipping boxes. For a copy of the catalog, write to Fluoroware Inc., Jonathan Industrial Center, Chaska, Minn. 55318 [426]



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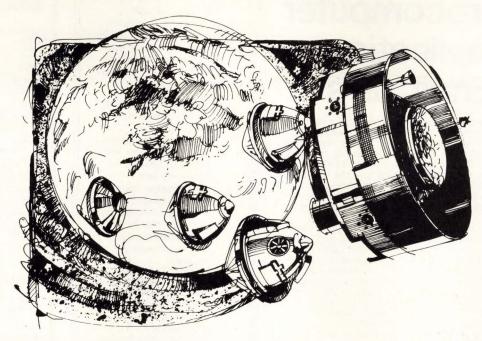
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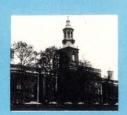
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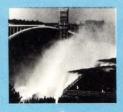
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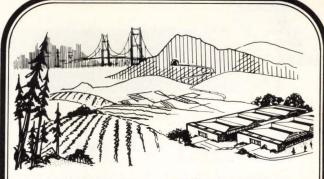
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When you plug into General Dynamics' Electronics Division, you get more than a challenging job, good pay and fringe benefits for you and your family. You get San Diego, one of the country's most beautiful cities. With miles of clean beaches, year-around golfing, sailing and tennis, and an average temperature of 68°, San Diego is one of America's most desired living areas.

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If your career needs challenge, stimulation or just a change of scenery, contact us immediately.

AUTOMATIC TEST EQUIPMENT

Automatic test equipment design including analog measurement, analog stimulus and digital subsystems.

Requires BSEE/MSEE and 2-5 years design experience. Analog design background preferred.

DISPLAY SYSTEMS DESIGN

Responsible for the configuration of display systems to meet customer requirements. Requires experience in areas of customer interface and proposal preparation, as well as display logic design or display analog circuit design.

ELECTROMAGNETIC COMPATIBILITY ENGINEER

Provide EMC support in development of electronic equipment and tracking navigation systems. Minimum of 2 years experience in system EMC analysis, EMC design, and equipment/system EMC testing is required; EMP and/or TEMPEST experience is desirable. Minimum BS degree with background in electromagnetic bonding.

RF DESIGN

Engineering specialist to head new airborne radar design group. Requires strong technical/proposal experience and analytical background. MSEE required.

Principal engineer for radar section requires technical/proposal and "hands on" experience. MSEE required.

HARDWARE/ SOFTWARE DEVELOPMENT

Work in field of digital image processing and display. Background in systems analysis such as error budget calculation helpful. Requires microprocessor familiarity and BSEE, Physics or Math degree.

DIGITAL DESIGN

Responsible for the design and special computer and transponder interfaces, display logic and microprocessor multifunction transponders used in sophisticated tracking systems.

All positions require at least a technical BS degree and 2-5 years experience.

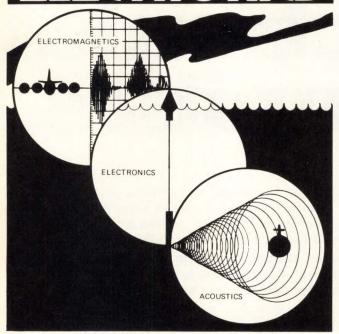
Excellent benefit program includes life insurance and medical program, dental and prescription drug plans, savings/stock investment and retirement plans.

Qualified applicants, submit your resume, including recent salary history, to: GENERAL DYNAMICS Electronics Division, Drawer KE, P.O. Box 81127, San Diego, CA 92138.

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IMMEDIATE OPENINGS:

Electronic Design Engineers - Responsible for the design of VHF-UHF receivers and transmitters, sonar receivers and transmitters, and various analog and digital circuits. Experience applicable to one or more of these areas required.

Mechanical Design Engineers - Responsible for the mechanical design of low-cost, high-quantity electromechanical and electronic equipment. Experience should include the design of injection moldings and die castings. Responsibilities consist of conceptual design, prototype build and qualification, and production support.

Call, or send resume and salary requirements to: Paul Cook, Employee Relations Manager



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BS or equivalent and electrical background. Minimum 4 years experience in Engineering Liaison, general design or both. Will prepare documentation of problems; analyze and write corrective action relating to documents or ENGINEERING ORDERS. Provide detail investigation and technical data or analysis on routine problems. Provide engineering assistance in various areas of manufacturing. Provide engineering interpretation for drawings and mock-up engineering guidance in fit and functional problems.

ELECTRICAL ELECTRONIC DESIGN

BS, MS, or equivalent, preferably in Electrical/Avionics design field. Minimum of 3-5 years of experience in aircraft electrical/avionics sub-system or component design. Perform specialized layouts and feasibility studies on highly complex installations and assemblies. Preparation of electrical lode analysis and responsible to review and check production documentation. These positions offer a salary commensurate with experience, an excellent benefits package, and the opportunity to work in one of Philadelphia's very attractive suburbs.

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The department head will report directly to the regional Telecommunications Division manager and within a few years will be responsible for about 100 employees. A qualified college degree and at least 5 years broad experience in Telecommunication or equivalent fields, such as digital techniques or composition, are considered essential for this assignment.

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ENGINEERS Working from detailed specifications capable of developing FORTRAN IV software modules. Executing under a mini-based real time operating system. Knowledge of Backus-Naur form of language definition a plus. BS Computer Science required.

SENIOR PROGRAMMER/ANALYSTS Using your familiarity with DBMS, be involved in design of application packages (TOTAL DBMS), research and design utilizing the DBMS theory, compiler, and language development and access methods. At least 2 years experience on a major DBMS system and overall experience not less than 4 years is needed, including scientific languages—FORTRAN, assembler, etc. BS in engineering, Math, Physics or CS of equivalent is essential, with higher degree preferred. Other disciplines will be considered if practical DP background is impressive.

PROGRAMMER/ANALYST Data communications person familiar with hardware/software. Capable of implementing network protocols

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PROJECT ENGINEERS • SENIOR ENGINEERS BSEE. 3-10 years experience with strong R&D background, hands-on experience current LSI and microprocessor technology, and leadership capability. Key positions in advanced development department, participation in state-of-the-art design activities.

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PROJECT ENGINEERS · SENIOR ENGINEERS · ENGINEERS

Responsibilities in these positions will be for engineering design and analysis of digital and analog circuitry, audio through microwave frequencies, with objective of translating circuit operation in computer programs for automatic fault detection and isolation. Background is essential in programming. ATE operation and circuit analysis, with at least 1-3 years experience in circuit design/analysis/development, 3-5 years in design and utilization of ATE and associated software. EE or Physics degree/equivalent is required.

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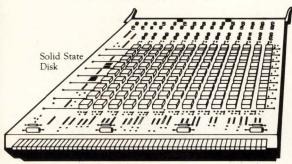
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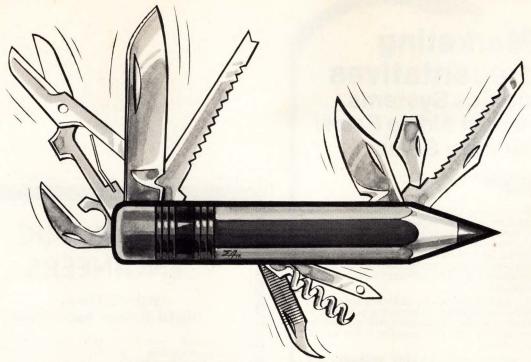
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